

Hadley17" Schematics Document

Haswell ULT

2013-06-24

REV :A00

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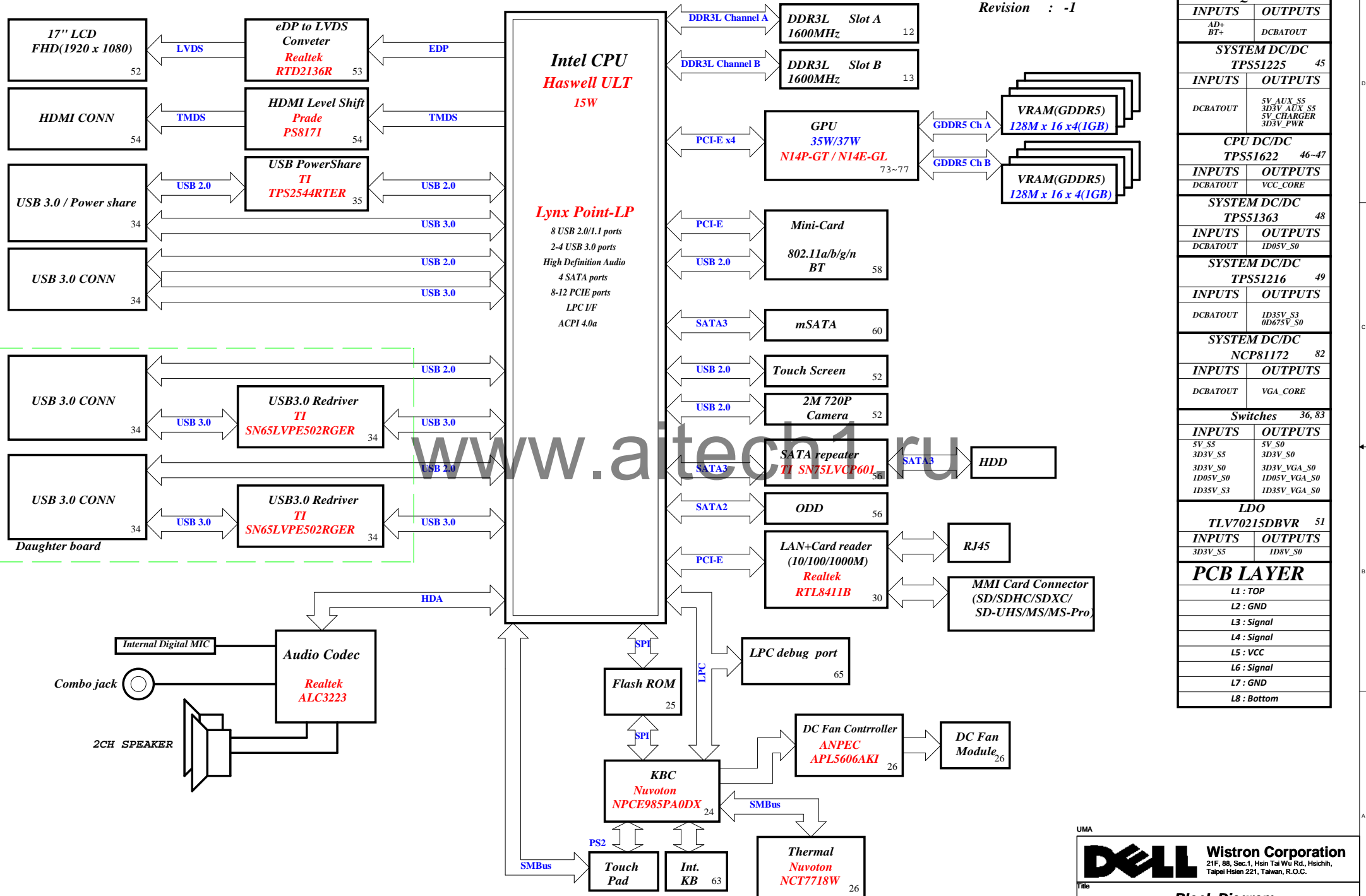
DY : None Installed

UMA

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size A3	Document Number Hadley 17"		Rev A00
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Hadley17 Block Diagram


Project code : 91.48L01.001
PCB P/N : 12309
Revision : -1



(Blanking)

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Title

(Reserved)

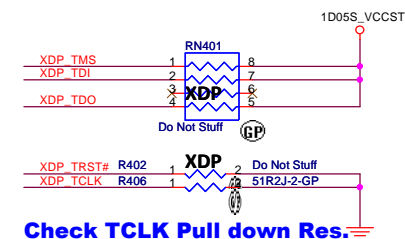
Size
A3

Document Number
Hadley 17"

Date: Tuesday, June 25, 2013

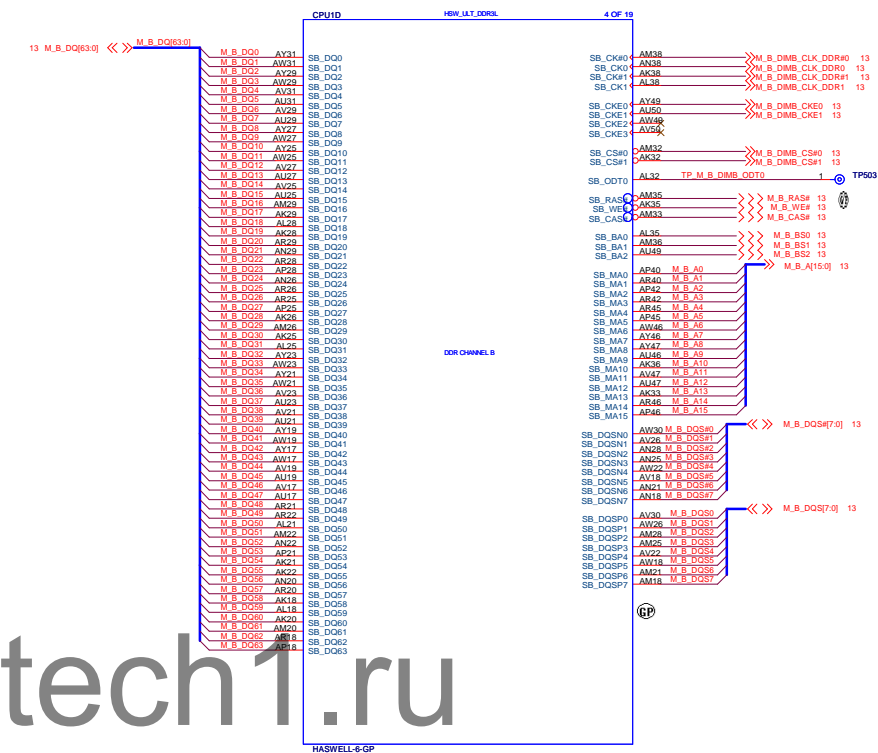
Rev
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Layout Note:
Design Guideline:
SM RCOMP keep routing length less than 500 mils.

- **Layout Note:**
Place close to DIMM



SSID = CPU

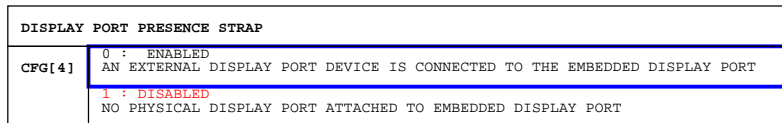
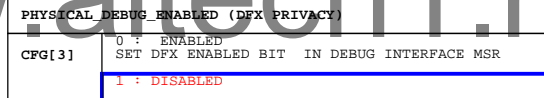


1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

CFG3

R604
Do Not Stuff

PHYSICAL DEBUG ENABLED (DFX PRIVACY)	
1	0 - Disabled



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Title	Author	Year	Journal	Volume	Page
...

CPU (RESERVED)

Size	A3
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Document Number

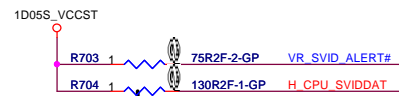
Hadley 17"

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SSID = CPU



1127 130R change to 110R
1203 110R change to 130R

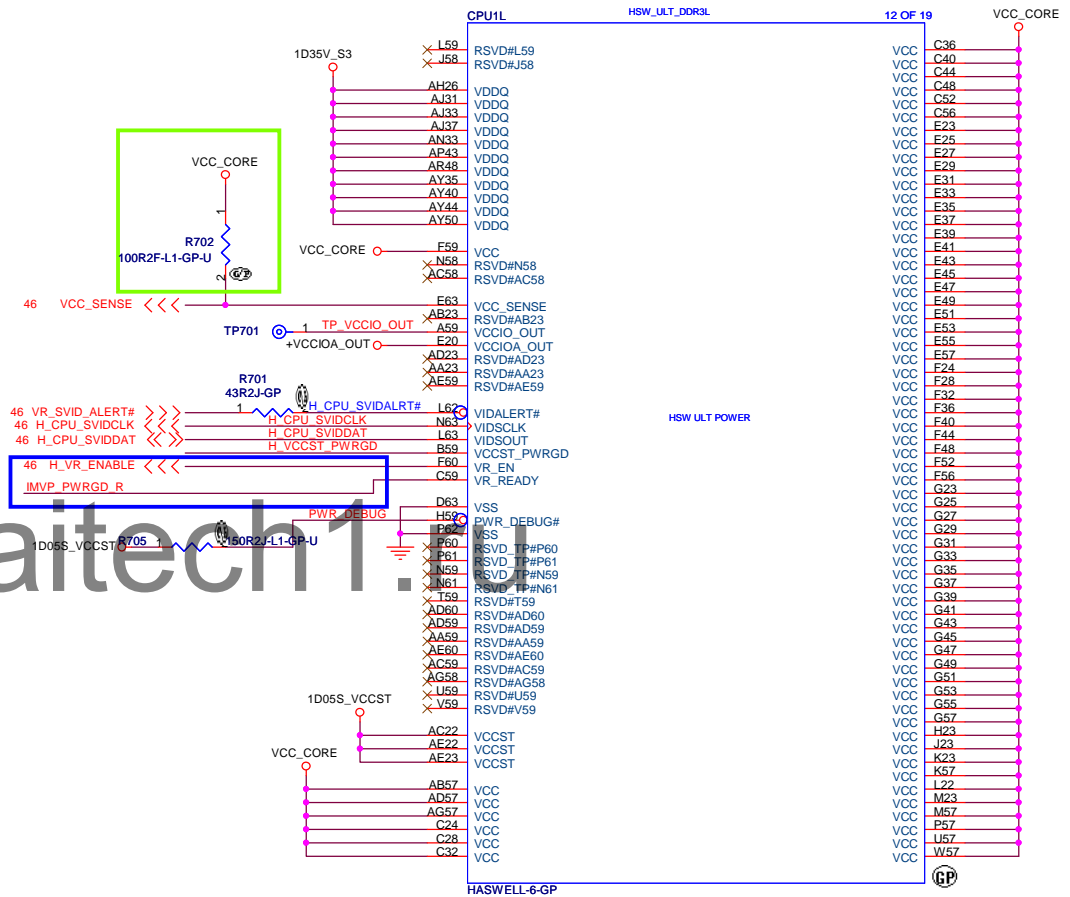
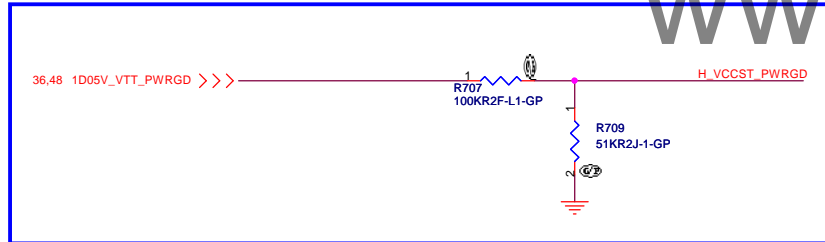
1109 Change net name of R703.2
from H_CPU_SVIDALRT# to
VR_SVID_ALERT#

Layout Note:

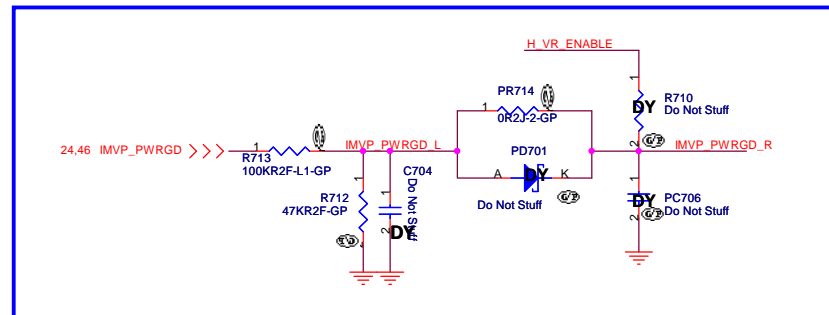
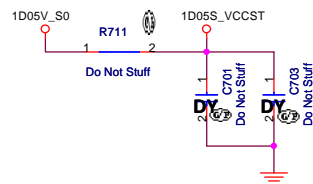
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE
impedance=50 ohm
3. Lwnlength match<25mil

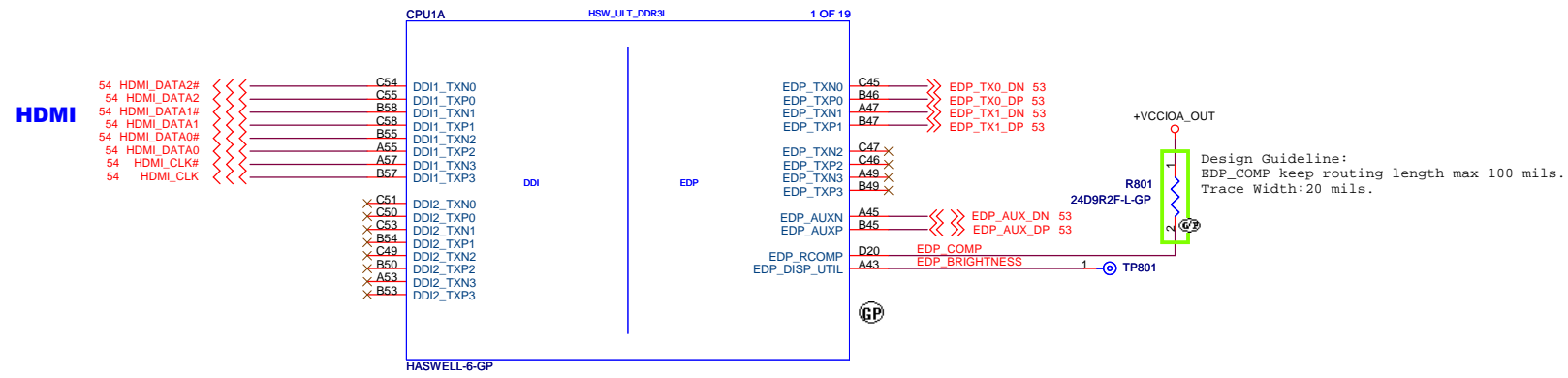
1109_modify for
power sequence

A00 0619



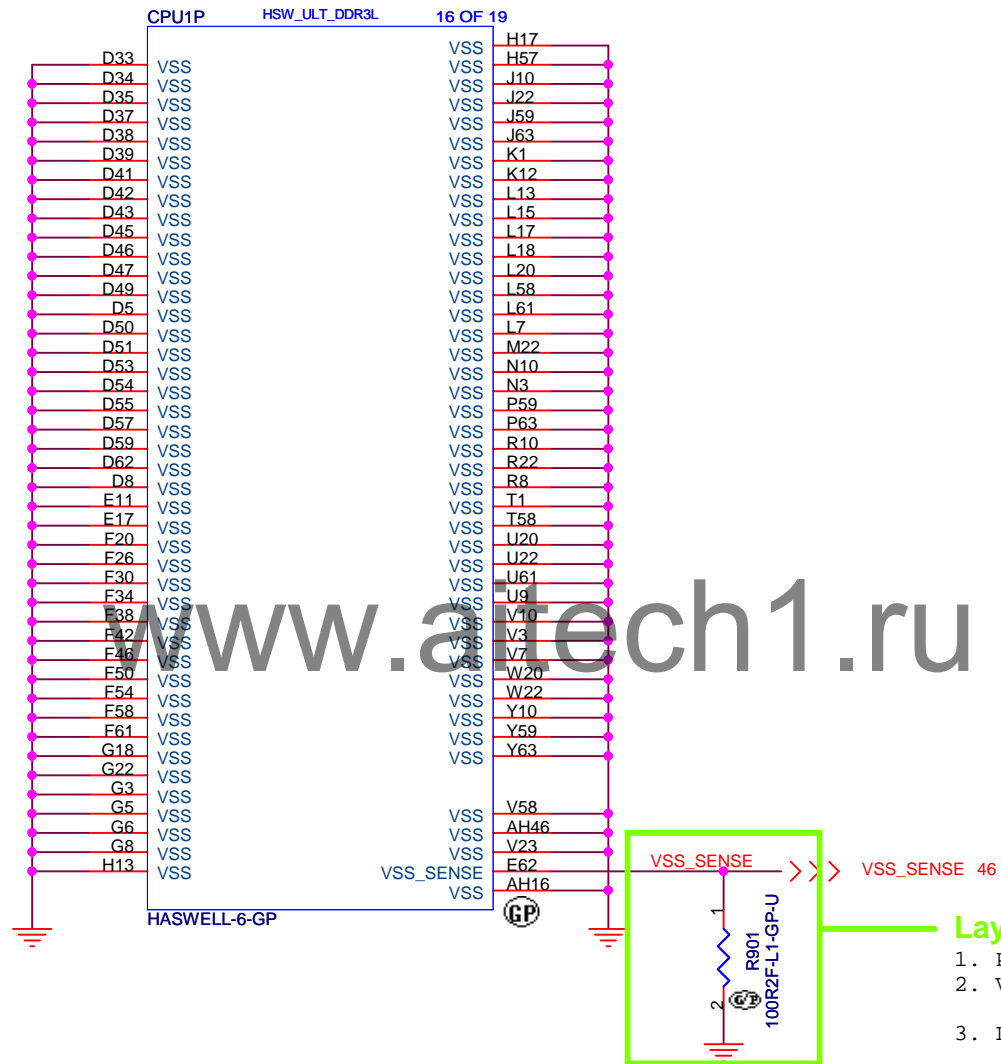
A00 0619






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SSID = CPU

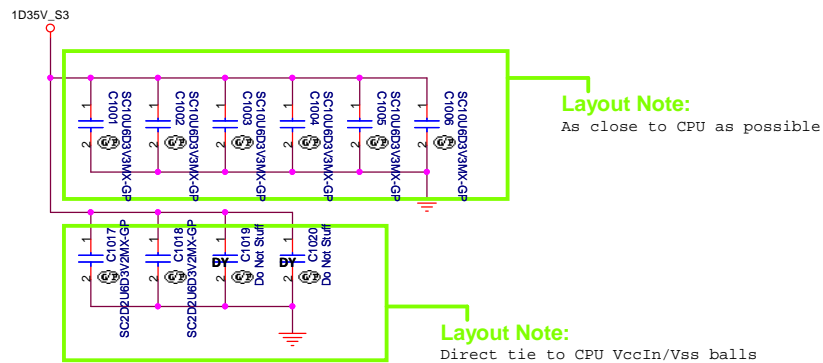


- Layout Note:**
- 1. Place close to CPU
 - 2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
 - 3. Lwnngth match<25mil

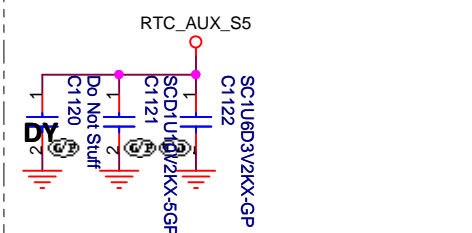
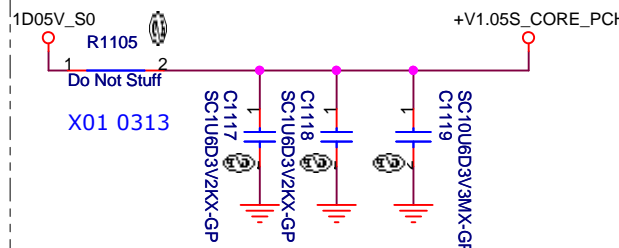
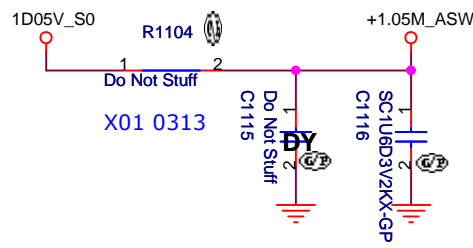
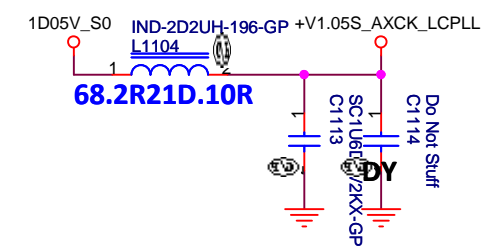
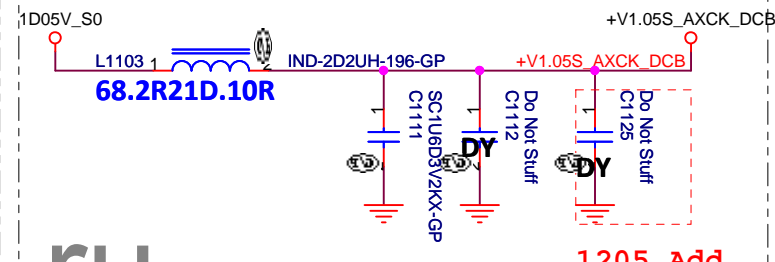
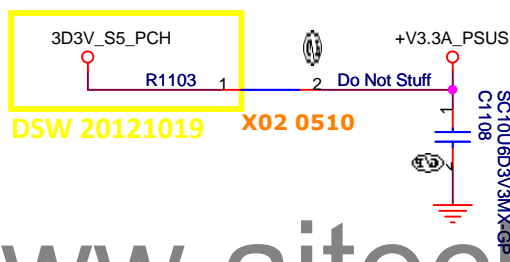
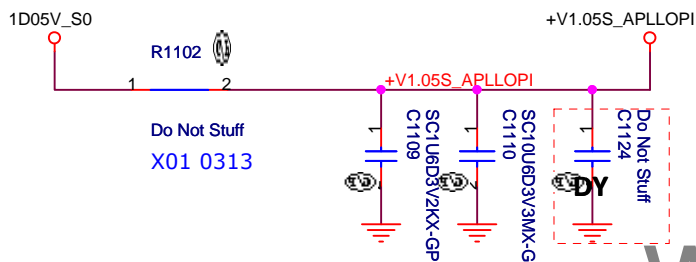
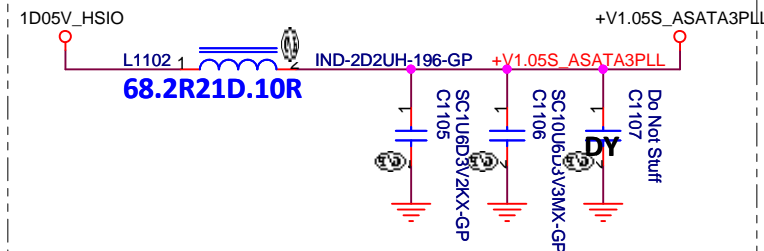
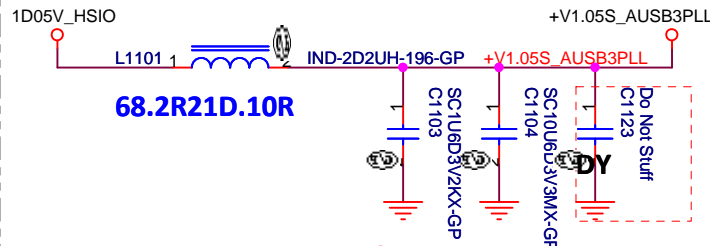
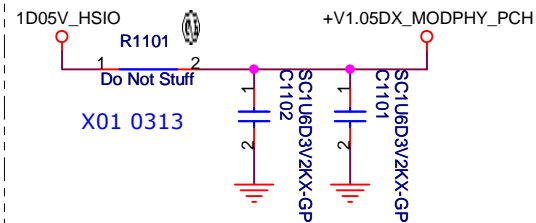
UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (VSS)			
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SSID = CPU



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Title

CPU(Power CAP2)

Size
A4

Document Number

Hadley 17"

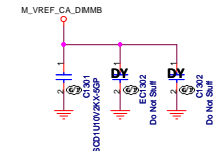
Rev
A00

Date: Tuesday, June 25, 2013

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Layout Note:

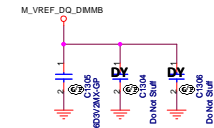
Place these caps close to VREF_CA



X02 0417
DY C1302 C1304 C1306, POP C1305 based on RMT test result.

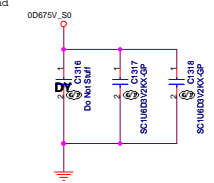
Layout Note:

Place these caps close to VREF_DQ



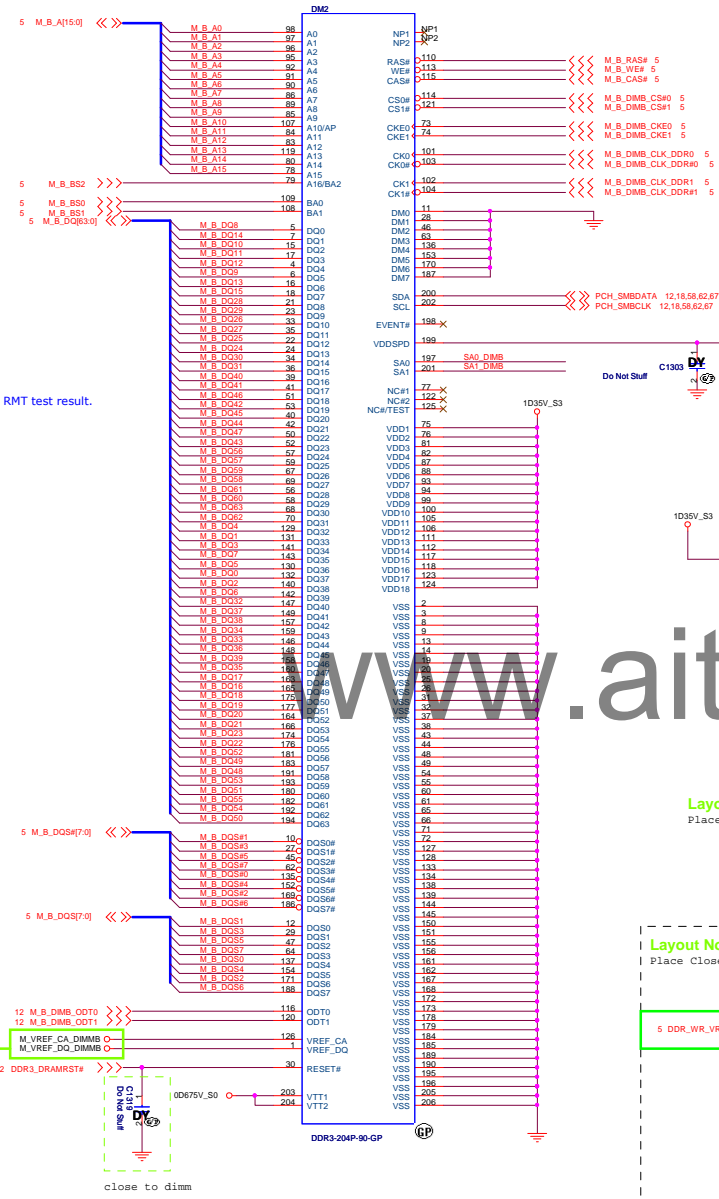
Layout Note:

Place these caps close to VTT1 and VTT2.



Layout Note:

All VREF traces should have width=20mil; spacing=20 mil

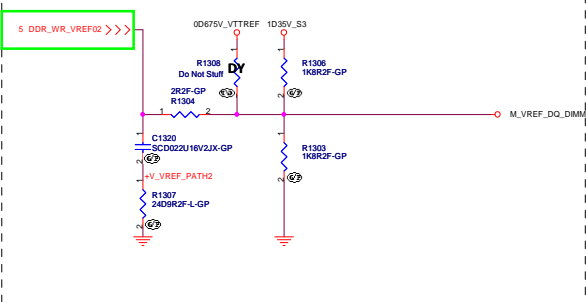


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Layout Note:
Place these Caps near SO-DIMMA.


Layout Note:

Place Close SO-DIMMA.



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Title

Size
A3

Document Number
M1&M3

Date: Tuesday, June 25, 2013

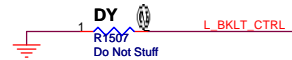
Rev
A00

Hadley 17"

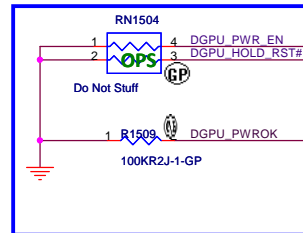
Sheet 14 of 102

SSID = CPU

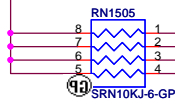
1204: Change R1507 PL 100K



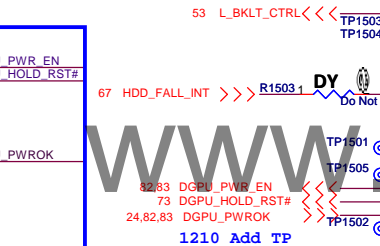
0102 Remove



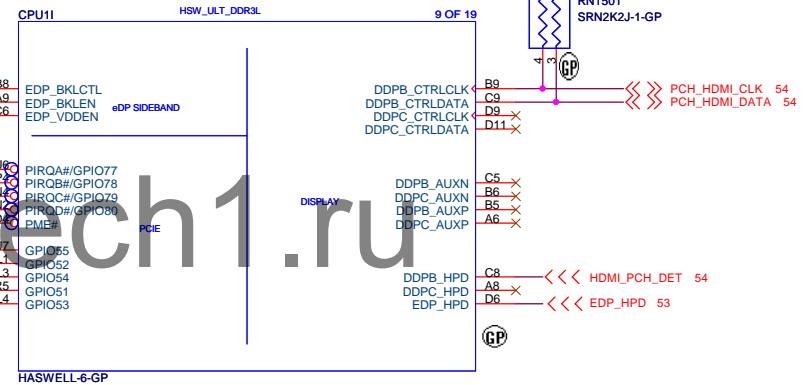
3D3V_S0



PIRQA#
PIRQC#



1210 Add TP

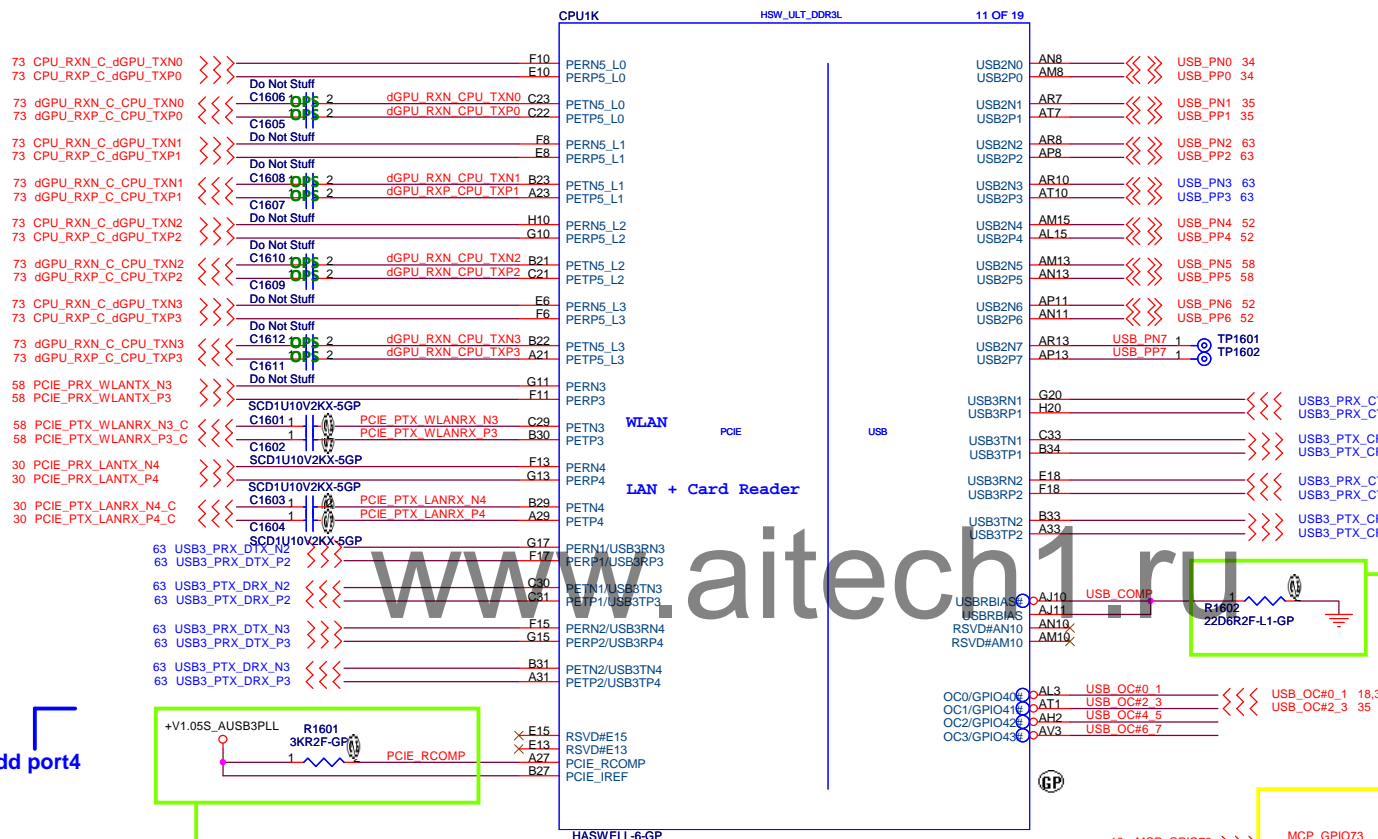


UMA

SSID = CPU

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	NC



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

1203 Add port4

Layout Note:

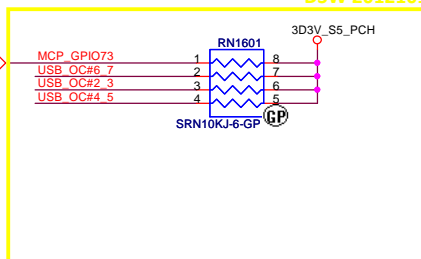
1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

PCIE Table

Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	LAN	
5(4lane)	TBD	
6(4lane)	TBD	SATA0~3

DSW 20121019

18 MCP_GPIO73 >>>



UMA

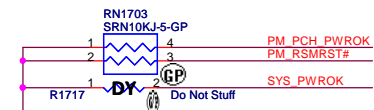


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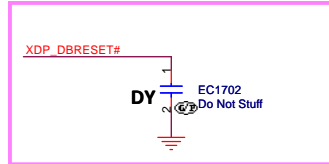
Title			CPU (PCIE/USB)	
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SSID = CPU

0116: modify for OBFF & wake up



0104:Reserve For EMI

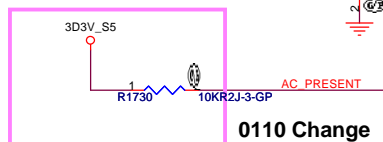
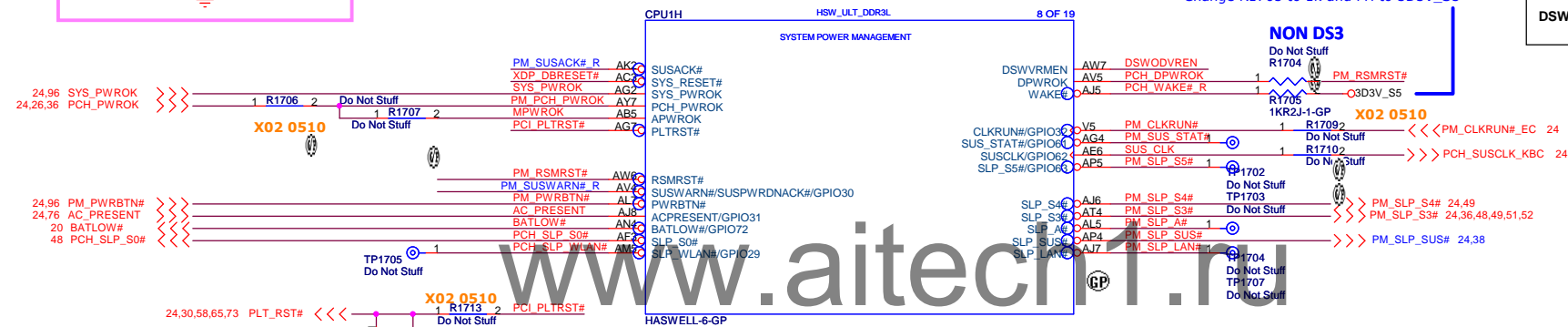
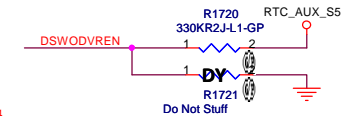


X01 0311
Remove OBFF circuit.

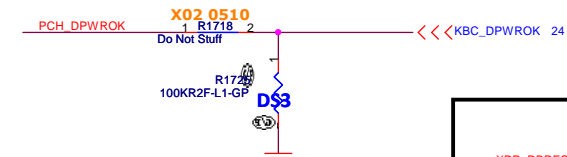
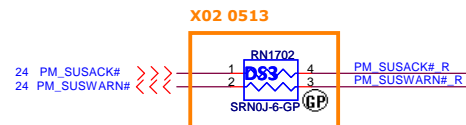
0117: Add R1722 to change Q1703 Gate Voltage To 13V

PCH strap pin:

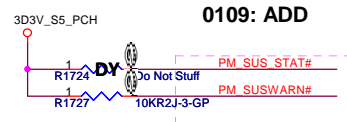
On Die DSW VR Enable	
DSWODVREN	Low = Disable * High = Enable (default)



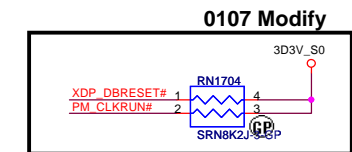
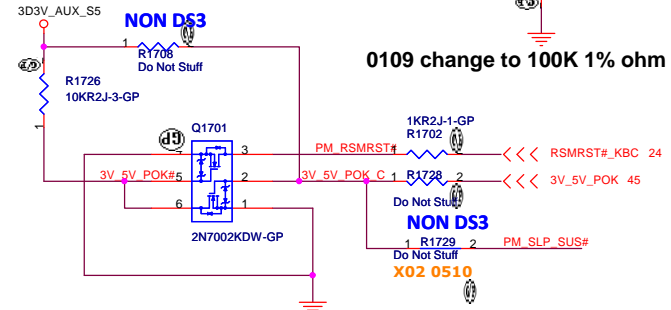
0110 Change



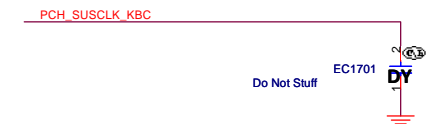
0109 change to 100K 1% ohm



0109: ADD



0107 Modify



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CPU (PM)

Hadley 17"

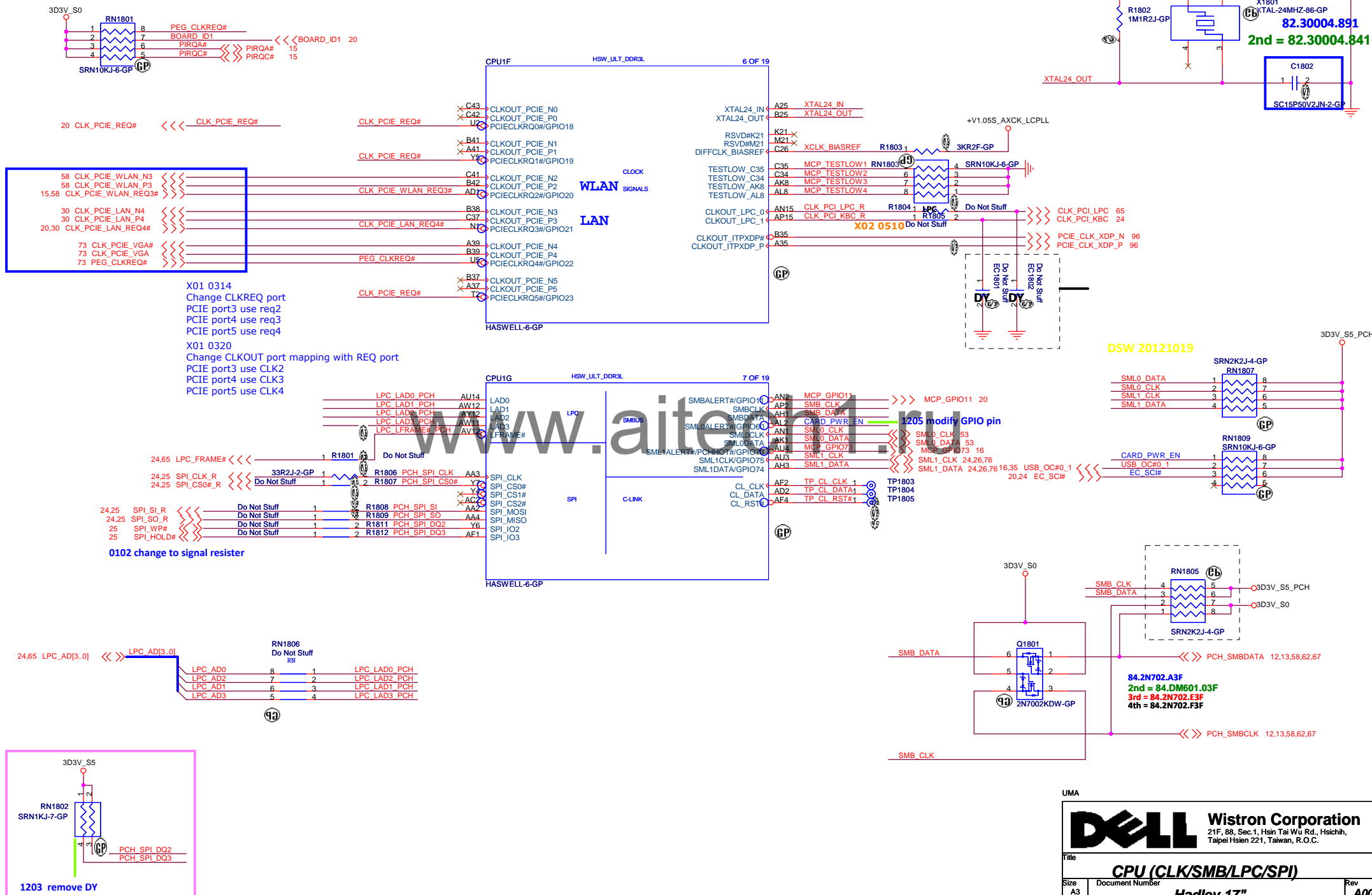
Size
A3

Document Number

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SSID = CPU



SSID = CPU

X01 0311

Add TP2004 and change net name to MCP_GPIO16.

15,67 FFS_INT2 >>> FFS_INT2

56 SATA_ODD_DA# >>> RTC_DET#

25 RTC_DET#

18 BOARD_ID1 <<< TP2002

21 HSIOPC <<< TP2020

24 EC_SWI# >>> EC_SWI#

18,24 EC_SCI# >>> EC_SCI#

56 HDD_DEVS_LP >>> MCP_GPIO70

60 MSATA_DEVS_LP >>> MCP_GPIO38

27 HDA_SPKR >>> MCP_GPIO38

1205 modify Net name

DSW 20121019

X02 0510

1210 Add

PCH strap pin:

NO REBOOT
HDA_SPKR
The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode (For A1 Stepping)

SDIO_D0 / GPIO66
Low = Disable "Top-Block swap" mode (Default)
High = Enable "Top-Block swap" mode

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

TLS Confidentiality

GPIO15
Low = Disable Intel ME Crypto TLS
High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS

Boot BIOS Destination
Low = SPI
High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
	0	0
	0	1
UMA	1	0
Optimus(NV)	1	1

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

1109 Add KB backlit GPIO pin

1219 Modify.EDS Update.

SW Suggest To Not Pop R2011 First.

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Title

CPU (GPIO)

Size

Document Number

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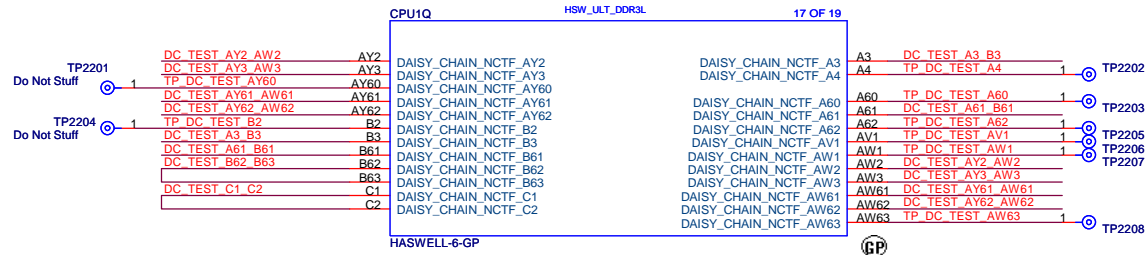
Rev

A00

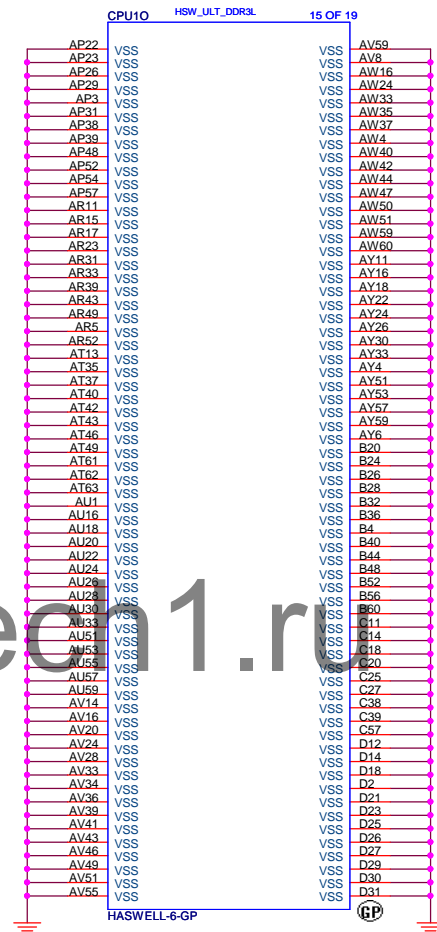
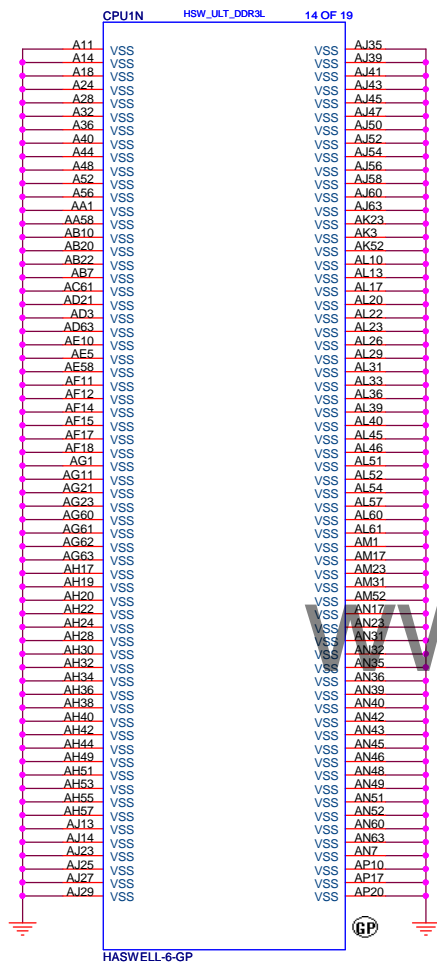
Date: Tuesday, June 25, 2013

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SSID = CPU



SSID = CPU

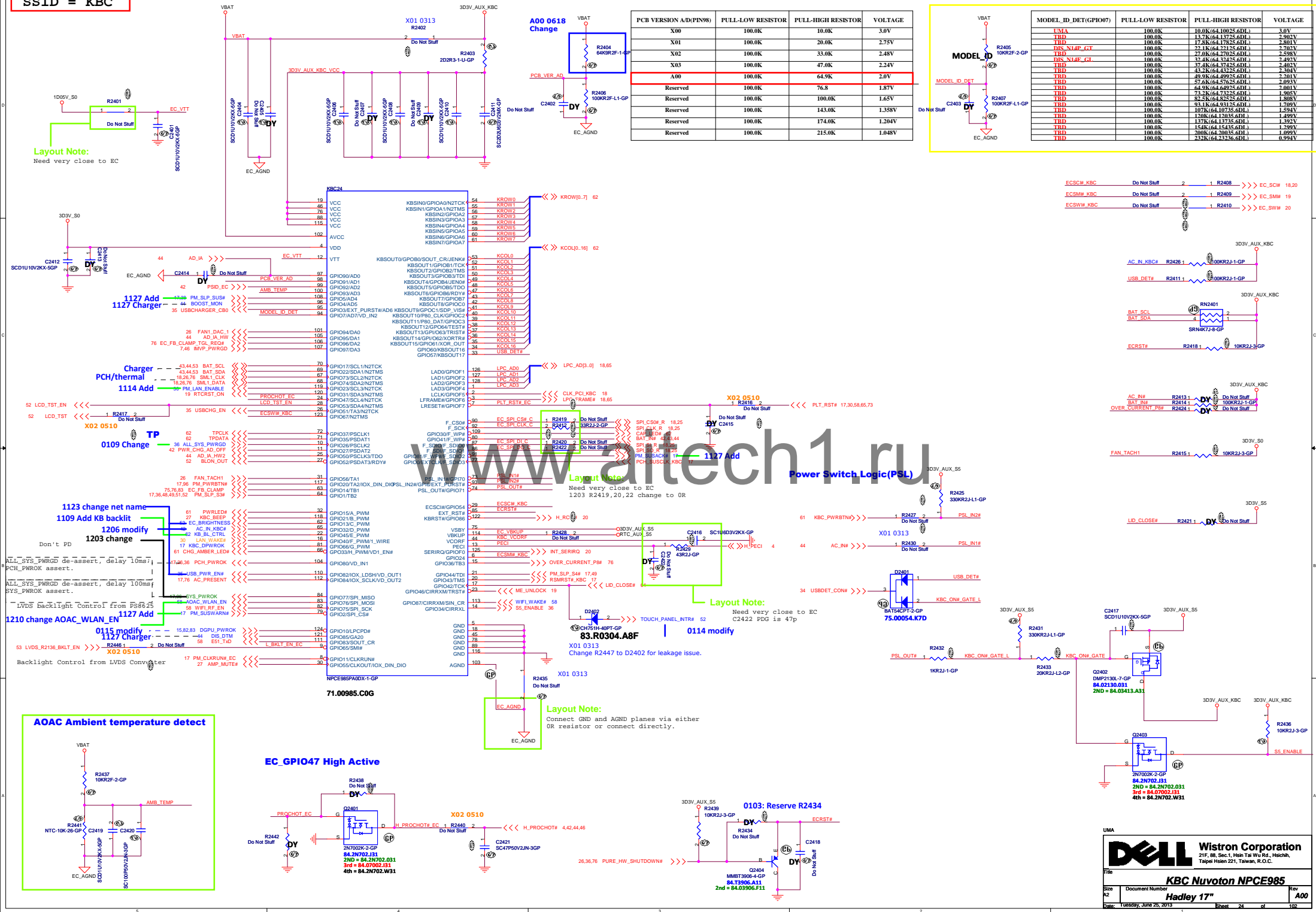


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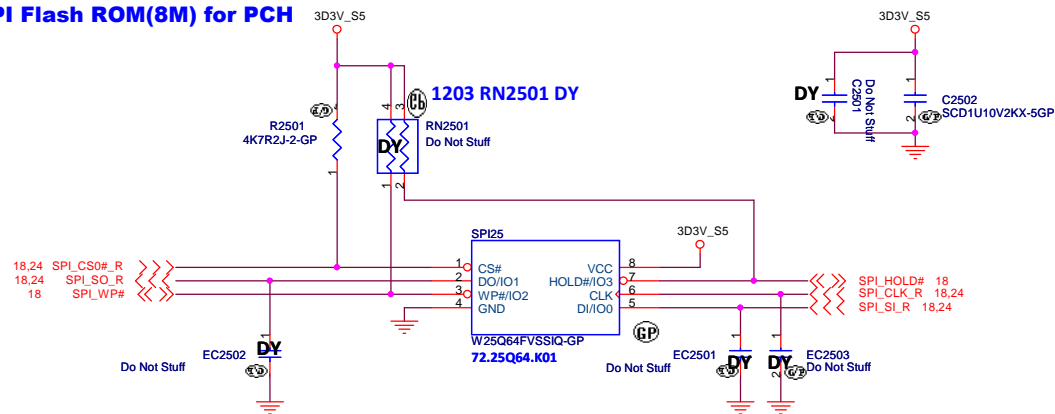
Title		
CPU (VSS)		
Size	Document Number	Rev
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SSID = KBC



SSID = Flash.ROM

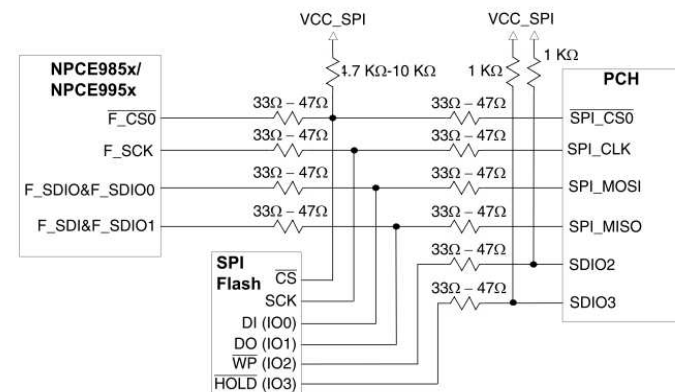
SPI Flash ROM(8M) for PCH



X01 0311
Remove SKT25.

Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o

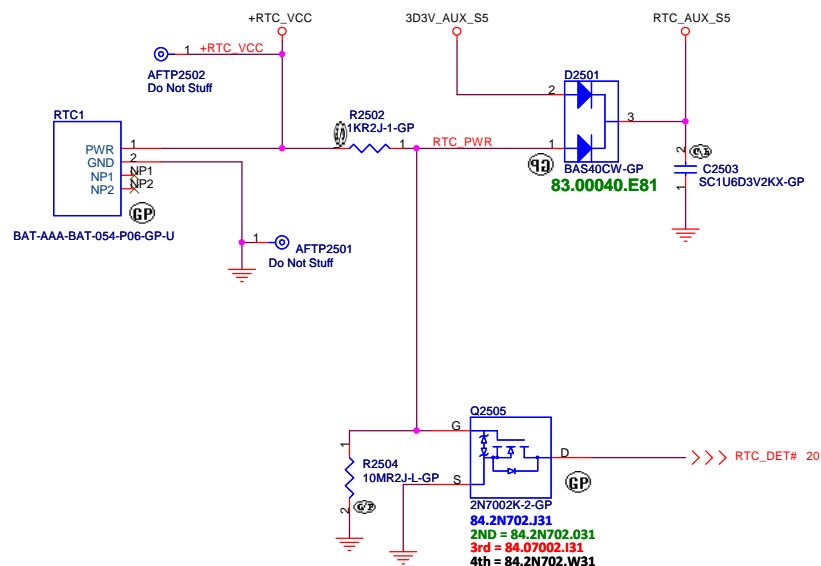
Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

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SSID = RBATT



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Title

Flash/RTC

Size

Document Number

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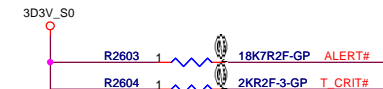
Rev

A00

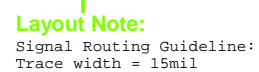
Date: Tuesday, June 25, 2013

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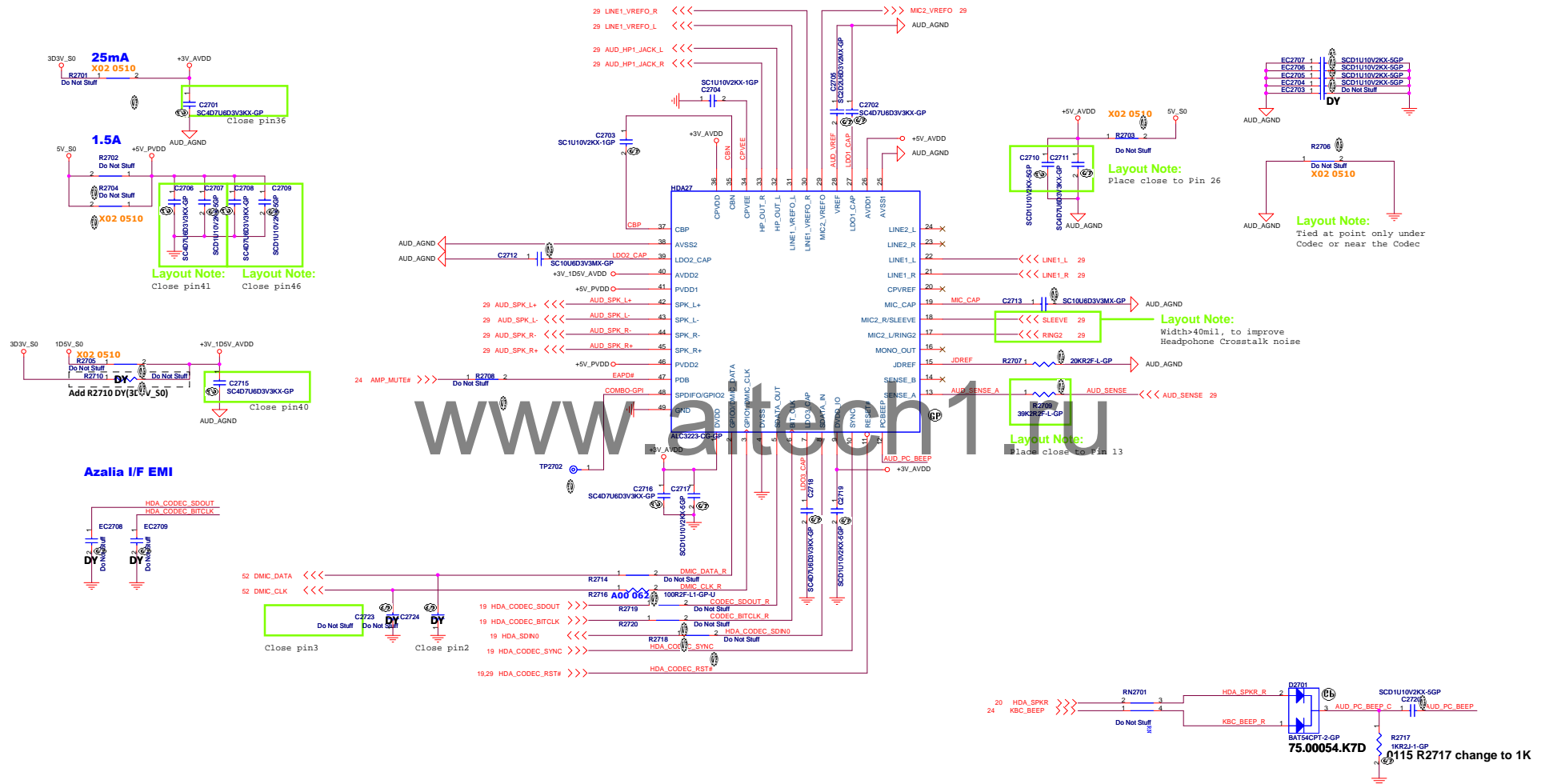
SSID = Thermal



Fan controller1




SSID = AUDIO



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Title

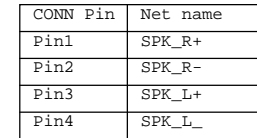
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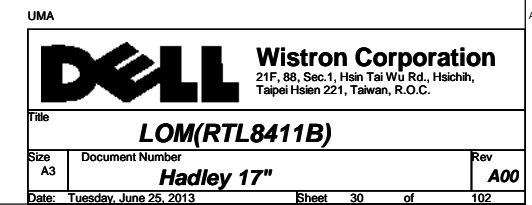
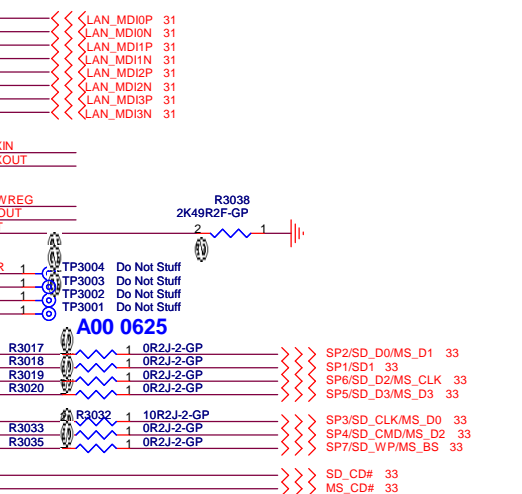
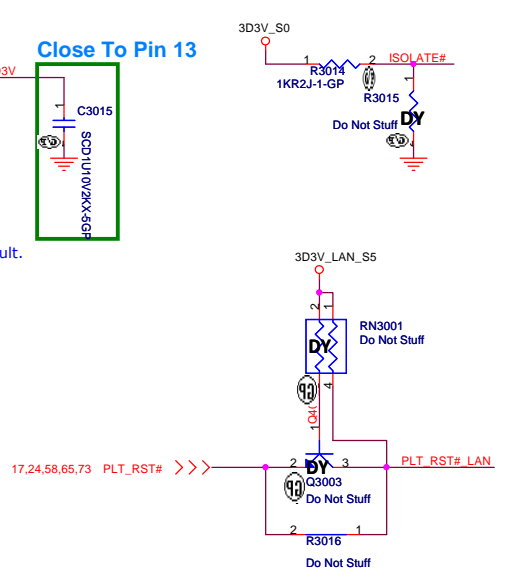
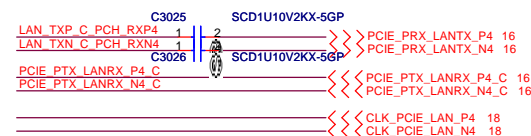
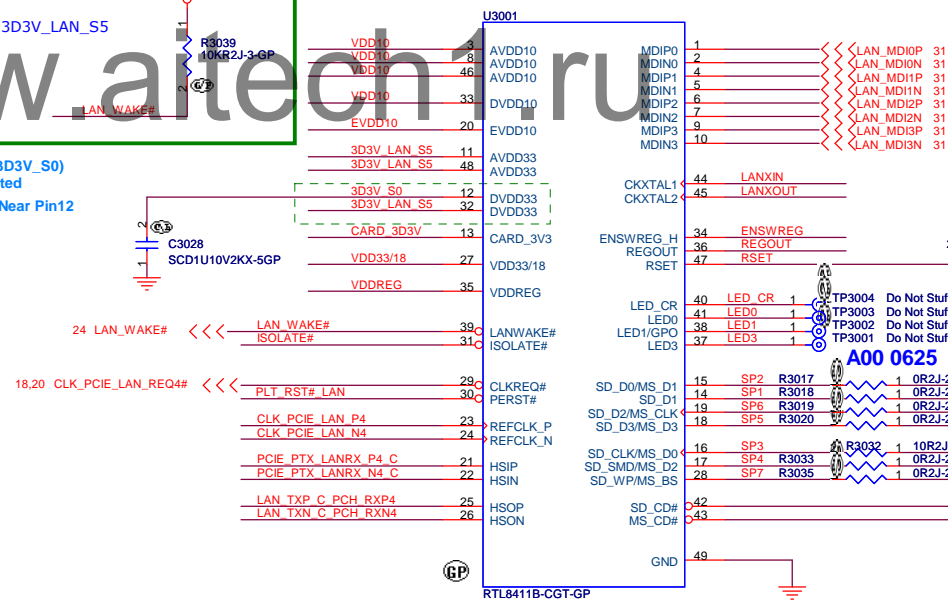
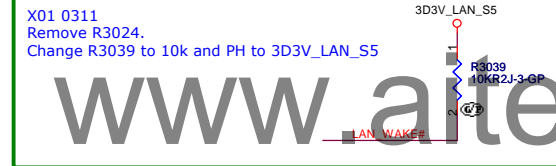
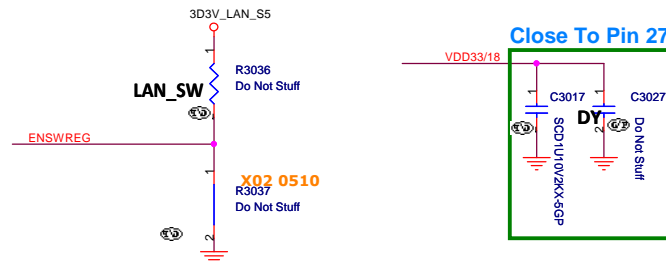
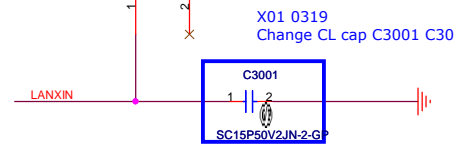
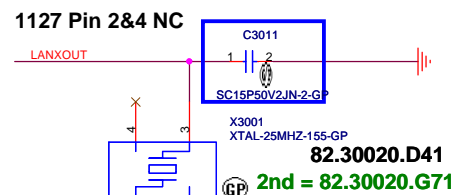
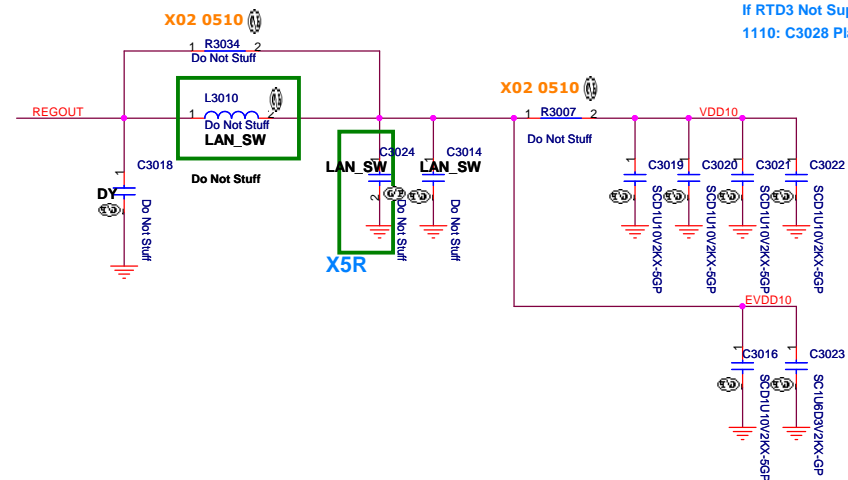
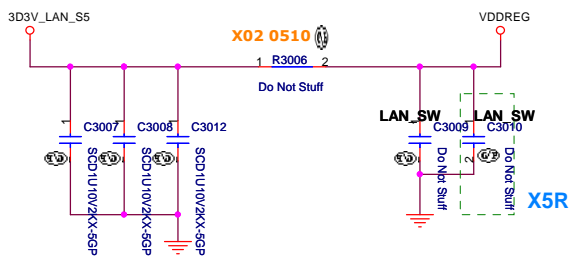
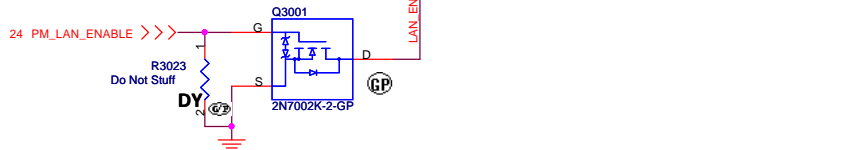
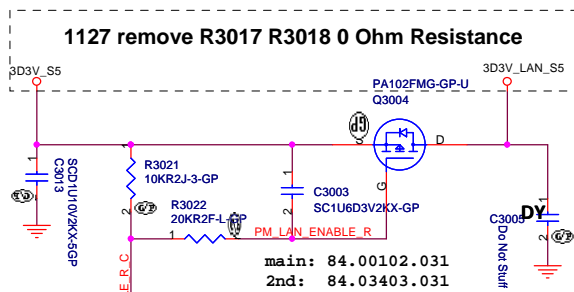
Rev
A00

Date: Tuesday, June 25, 2013

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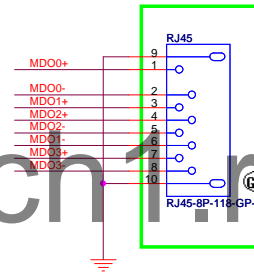
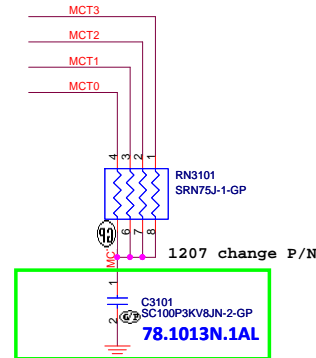
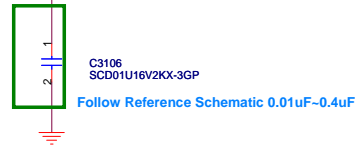
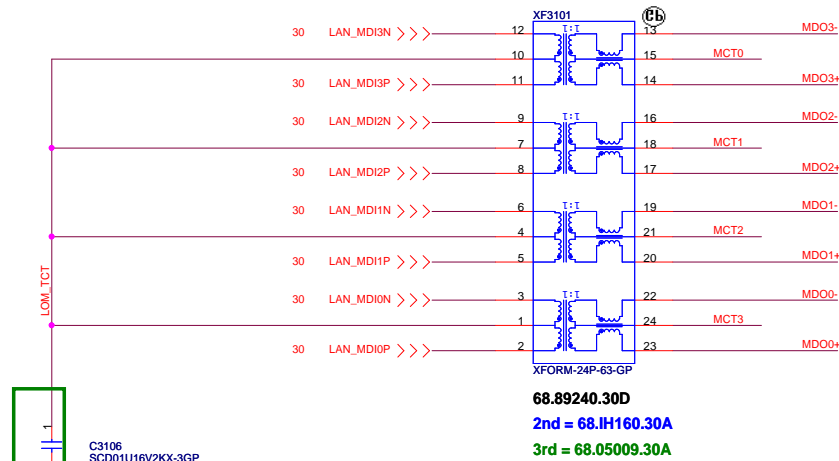


LAN CHIP



SSID = LOM

GIGA LAN Transformer



Layout:
Place near RJ45

AFTP3107	1	MDO0+
AFTP3102	1	MDO0-
AFTP3101	1	MDO1+
AFTP3103	1	MDO2+
AFTP3104	1	MDO2-
AFTP3106	1	MDO1-
AFTP3105	1	MDO3+
AFTP3108	1	MDO3-


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Title			
RJ45+Transformer			
Size	Document Number	Rev	
Custom			A00
Date:	Tuesday, June 25, 2013	Sheet	31 of 102

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Title

Size
A3

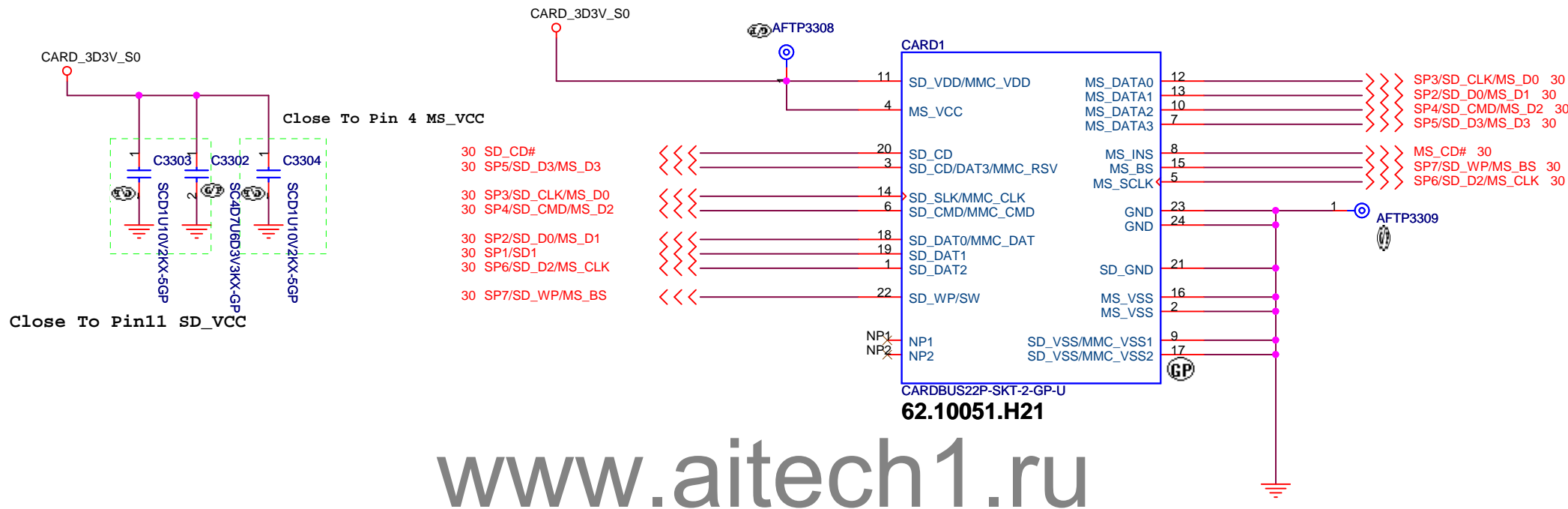
Document Number
Hadley 17"

Rev
A00

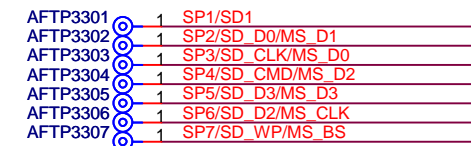
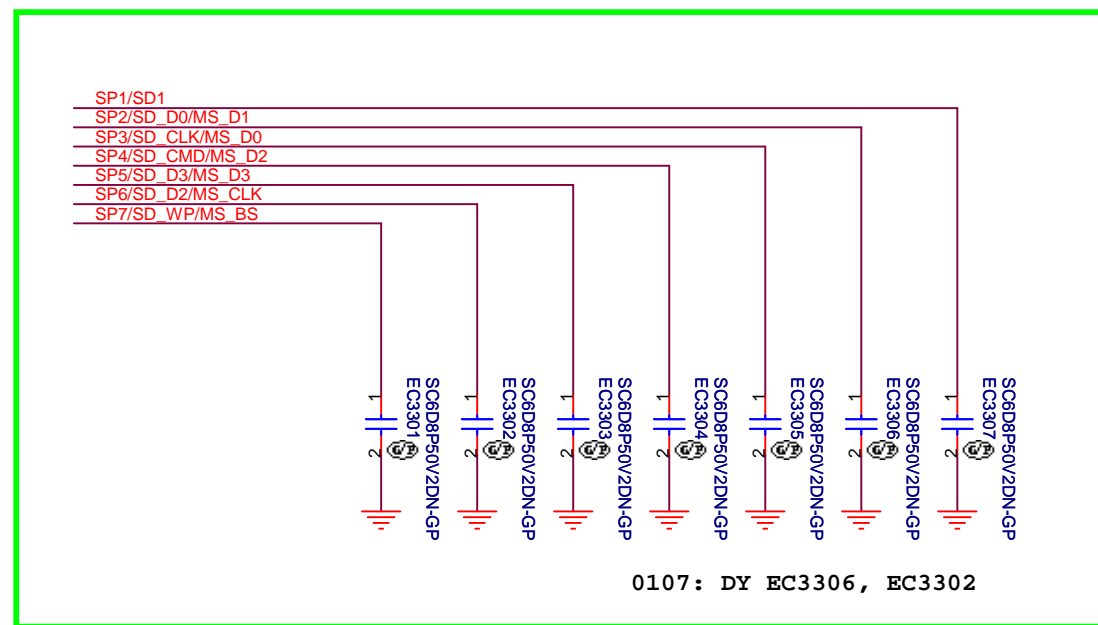
Date: Tuesday, June 25, 2013

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SSID = SDIO



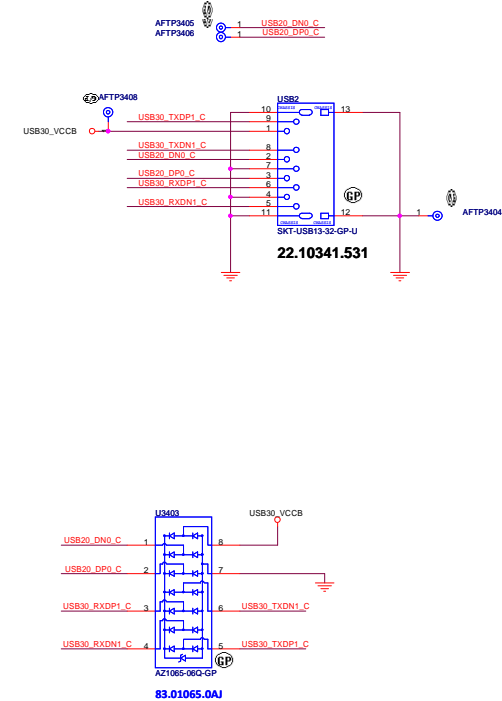
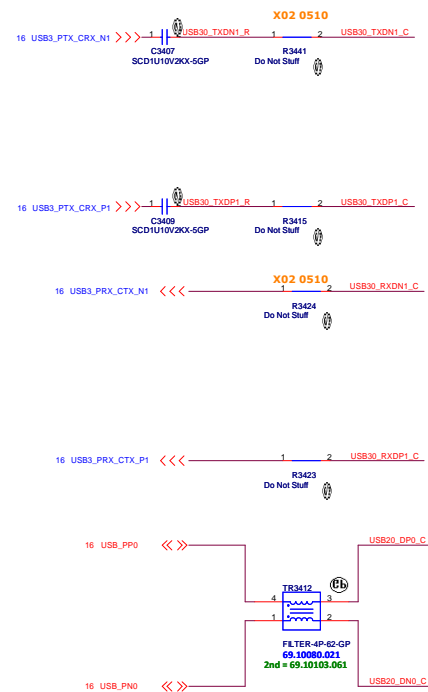
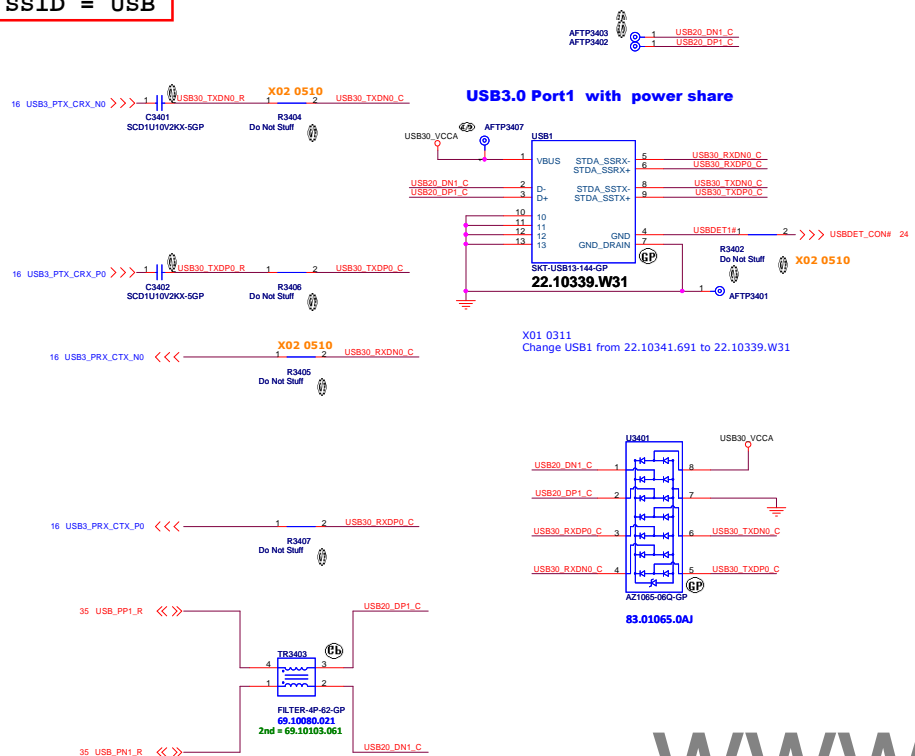
Reserve EMI Cap, CLK Pop



UMA

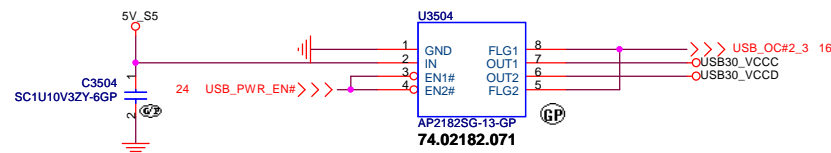
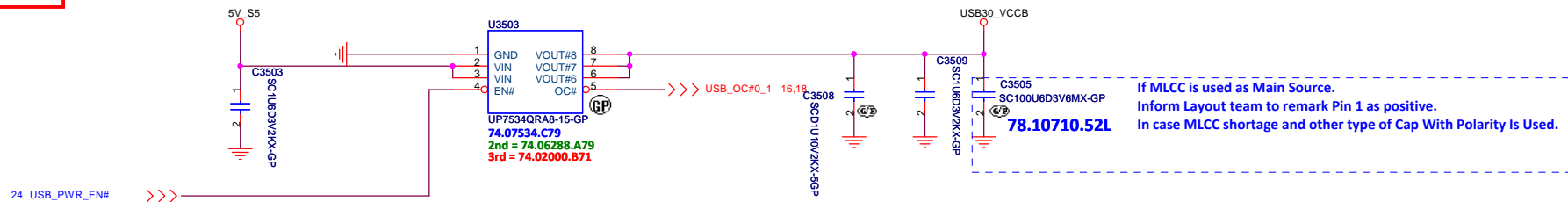
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Card Reader CONN			
Size A4	Document Number Hadley 17"		Rev A00
Date: Tuesday, June 25, 2013		Sheet 33 of	102

SSID = USB

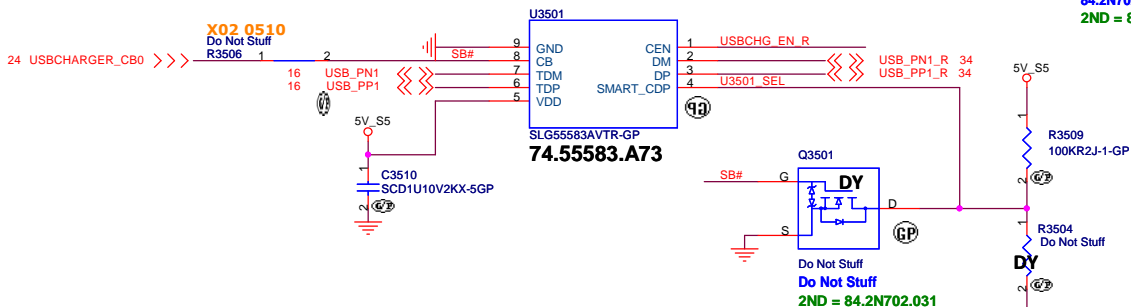


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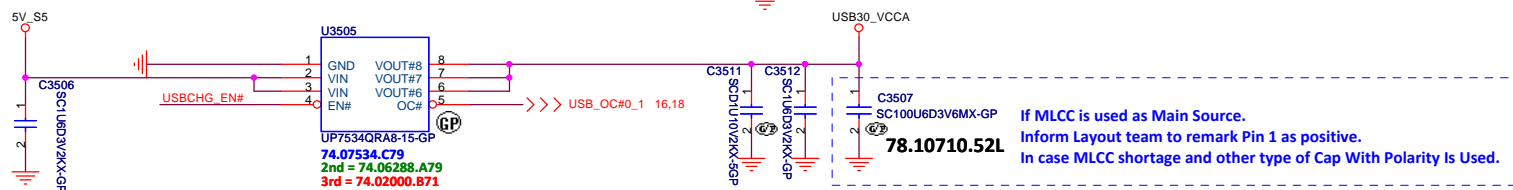
SSID = USB



X01 0320
Modify USB charger circuit.



SB/ (pin 8)	SEL(pin 4)	Feature	pin 1 role (INT or INT/)
0	0	Auto S & C without mouse/keyboard pass through	INT or INT/
0	1	Auto S & C with mouse/keyboard pass through	INT or INT/
1	0	S0 charging with SDP only	INT or INT/
1	1	S0 charging with CDP or SDP only (depending on external device)	INT or INT/
0	M = (1/2)*V _{DD}	Test Mode, M = V _{DD/2} = (1/2)*V _{DD}	



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Title

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Rev A00

Power Good

ROSA Run Power



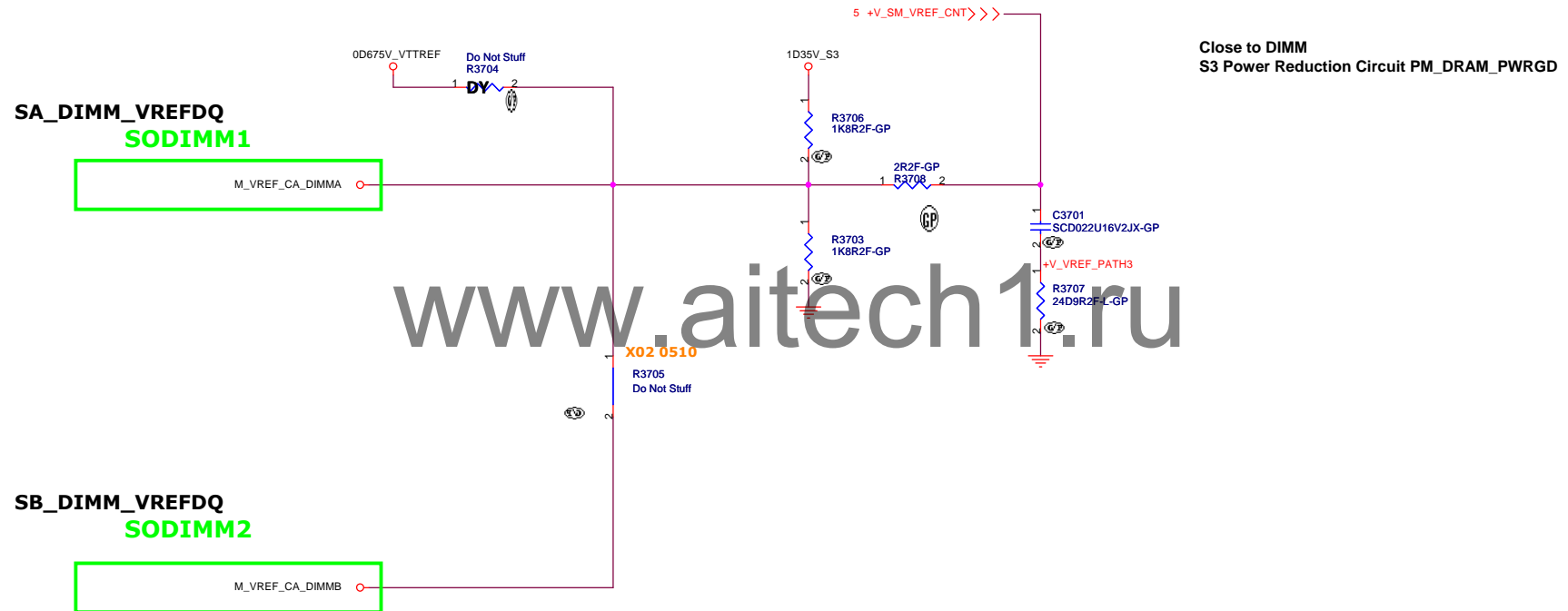
Power Plane Enable

Hadley 17"

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SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMMA.




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Title

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A3

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Hadley 17"

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A00


Date: Tuesday, June 25, 2013

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Title

Size
A3

Document Number
Reserved
Hadley 17"


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A00

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Title

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Size
A3

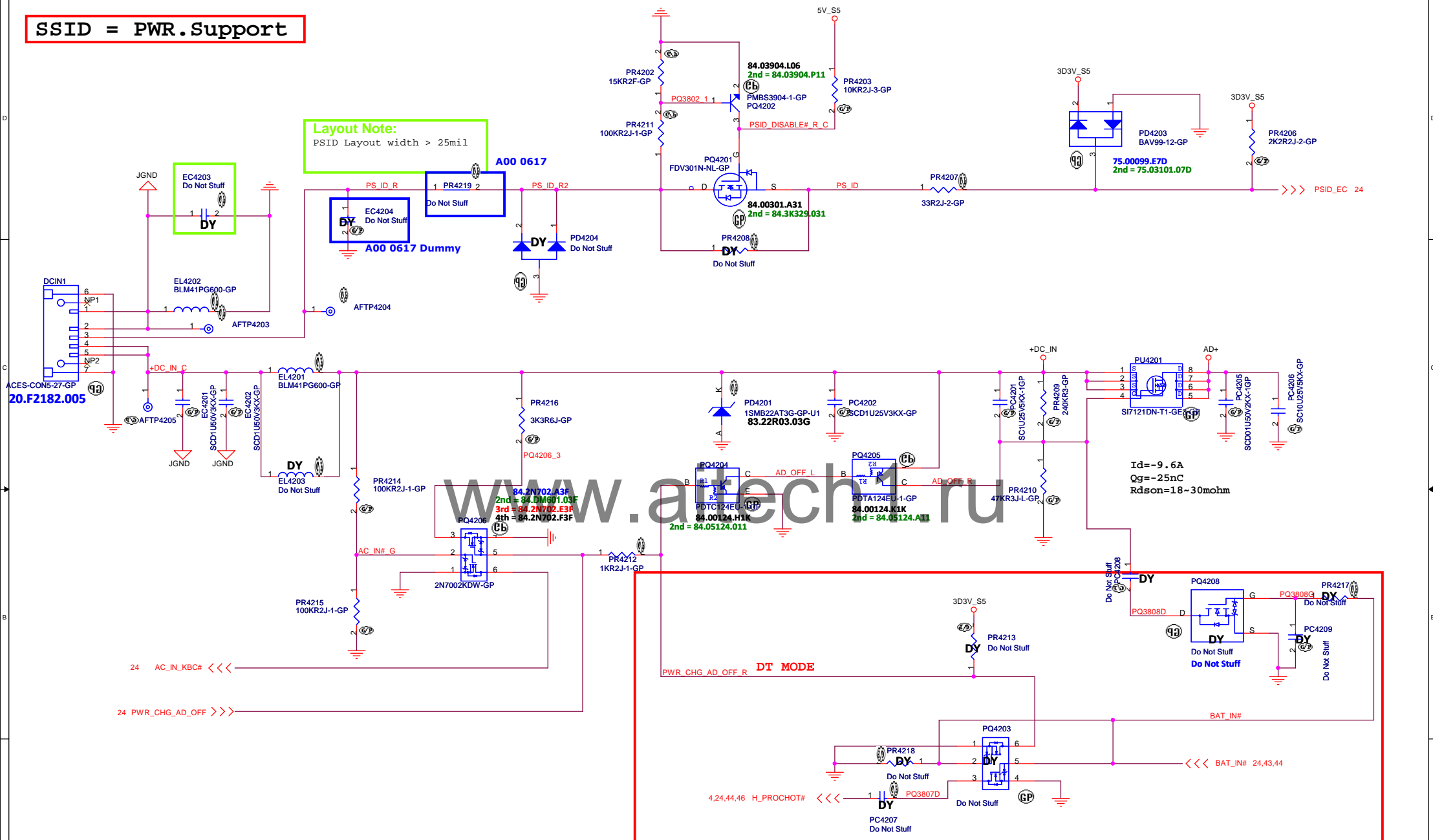
Document Number
Hadley 17"

Rev
A00

Date: Tuesday, June 25, 2013

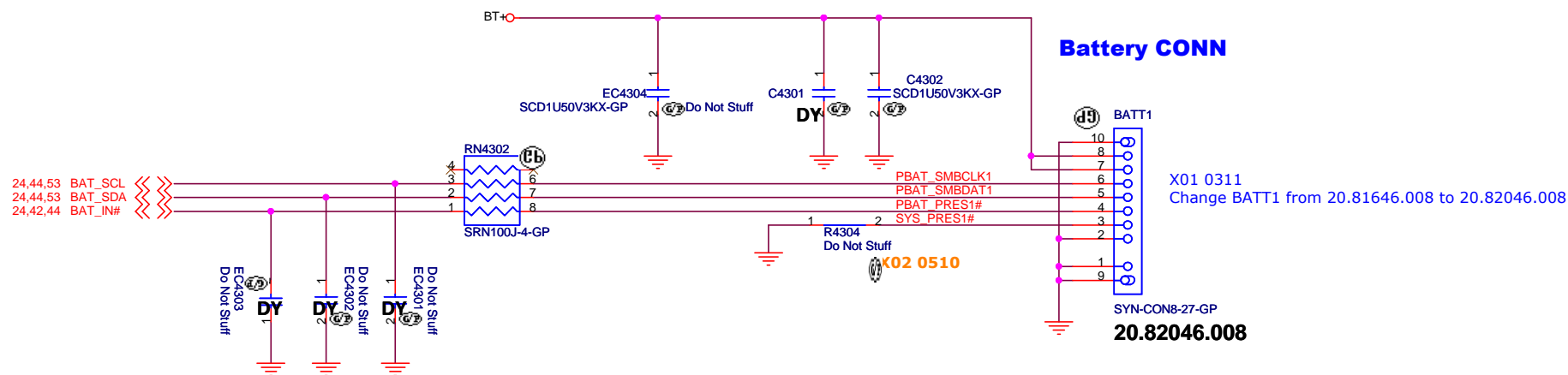
Sheet 41 of 102

SSID = PWR.Support

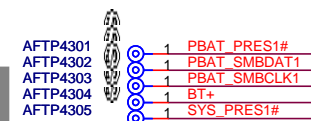


0109: DY DT MODE, End User Can't Remove Battery

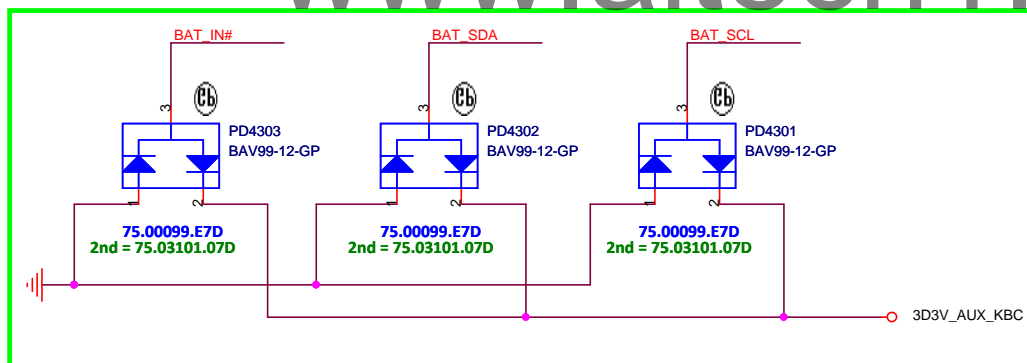
SSID = PWR.Support



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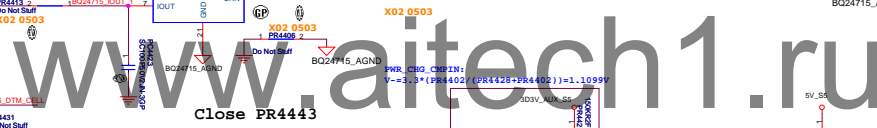


Layout Note:
Place near Battery CONN



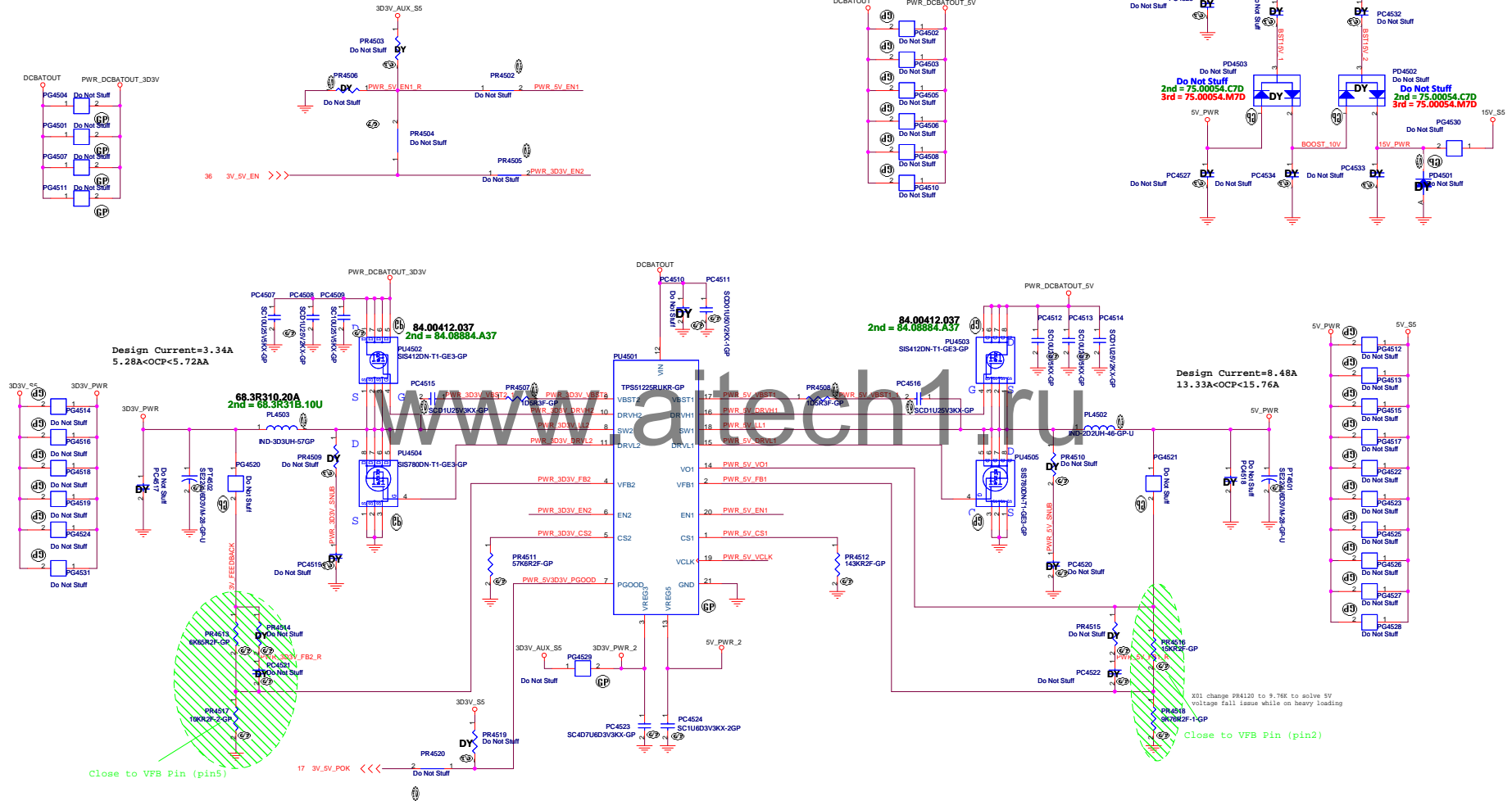
UMA

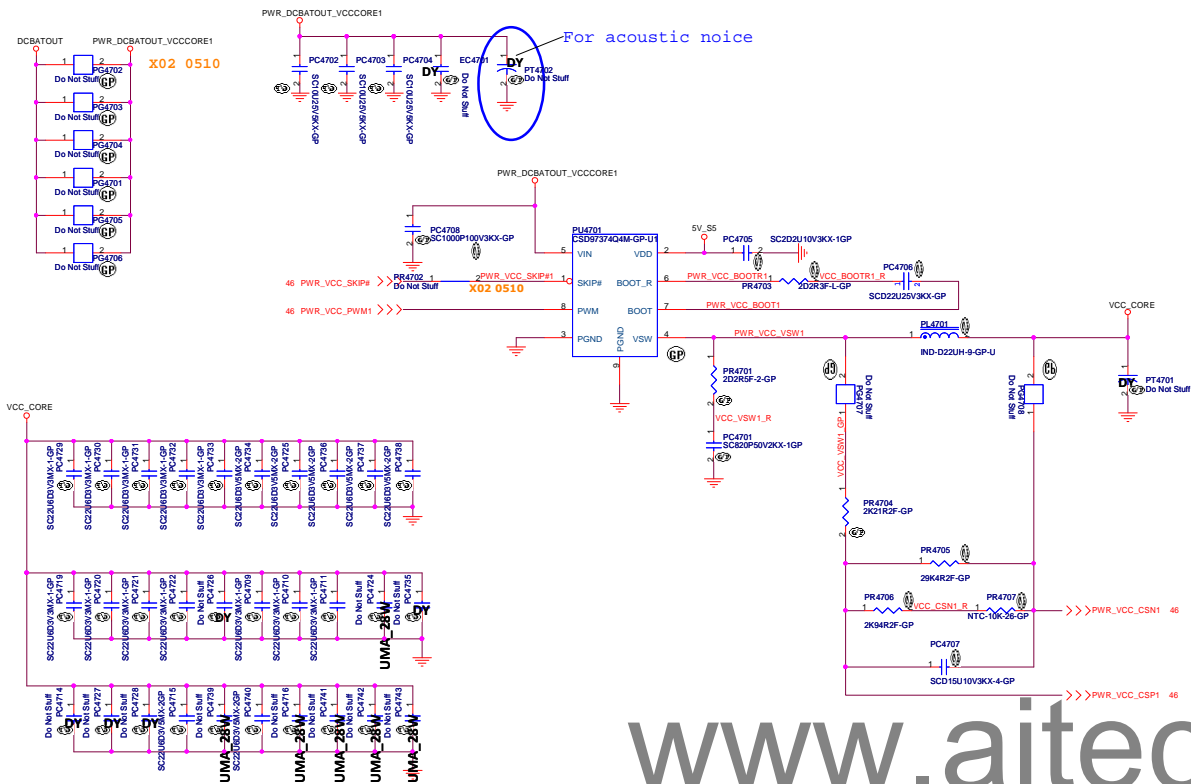
DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BATT CONN			
Size	Document Number		Rev
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ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	2.248V
65W	H	L	1.736V
45W	L	H	1.324V

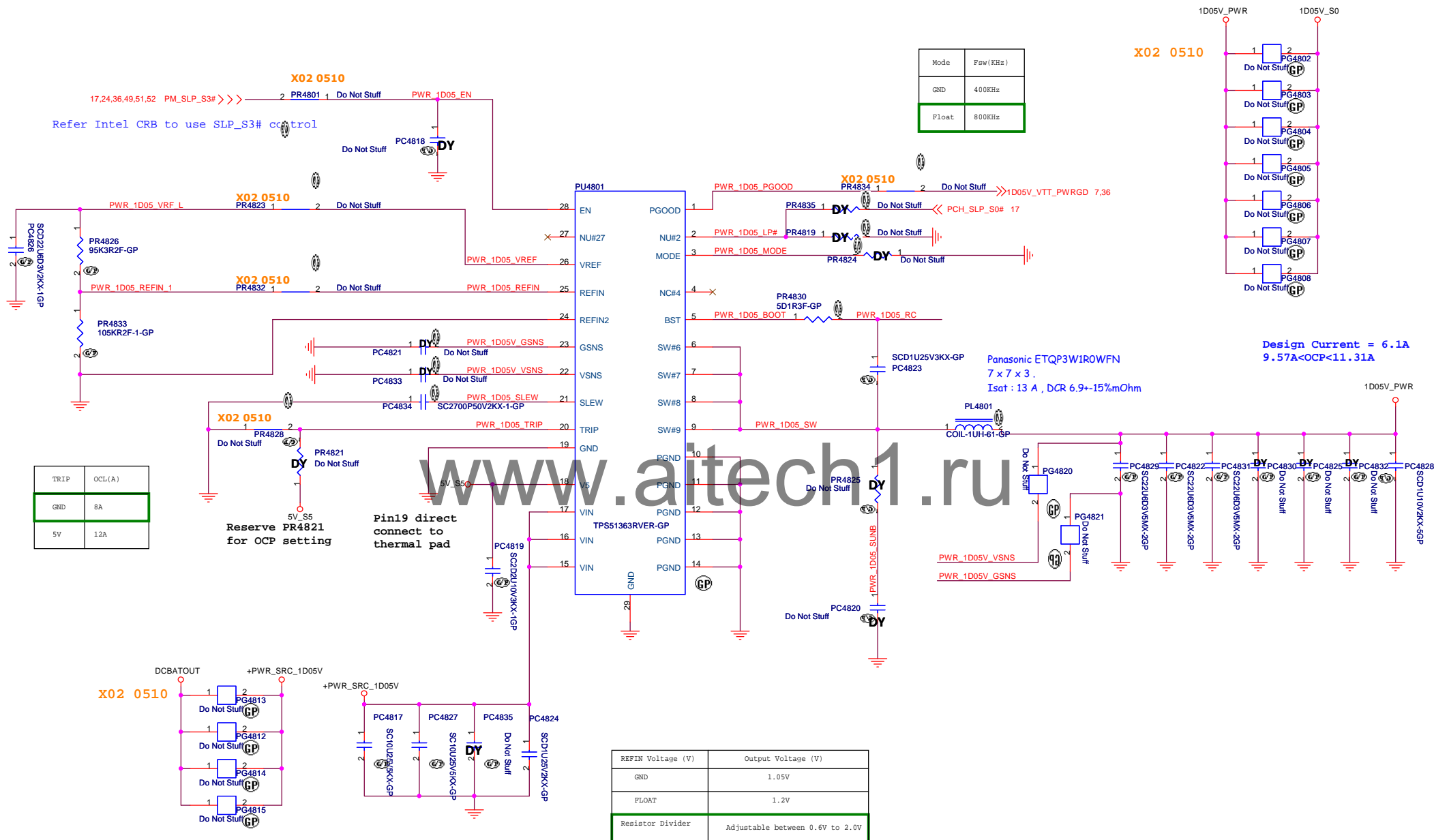
SSID = PWR.Plane.Regulator_5v3p3v





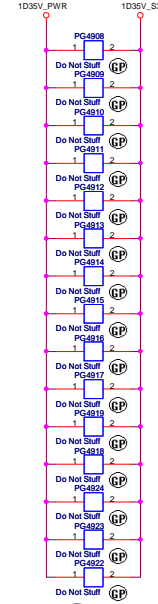
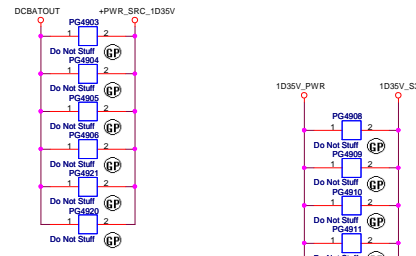
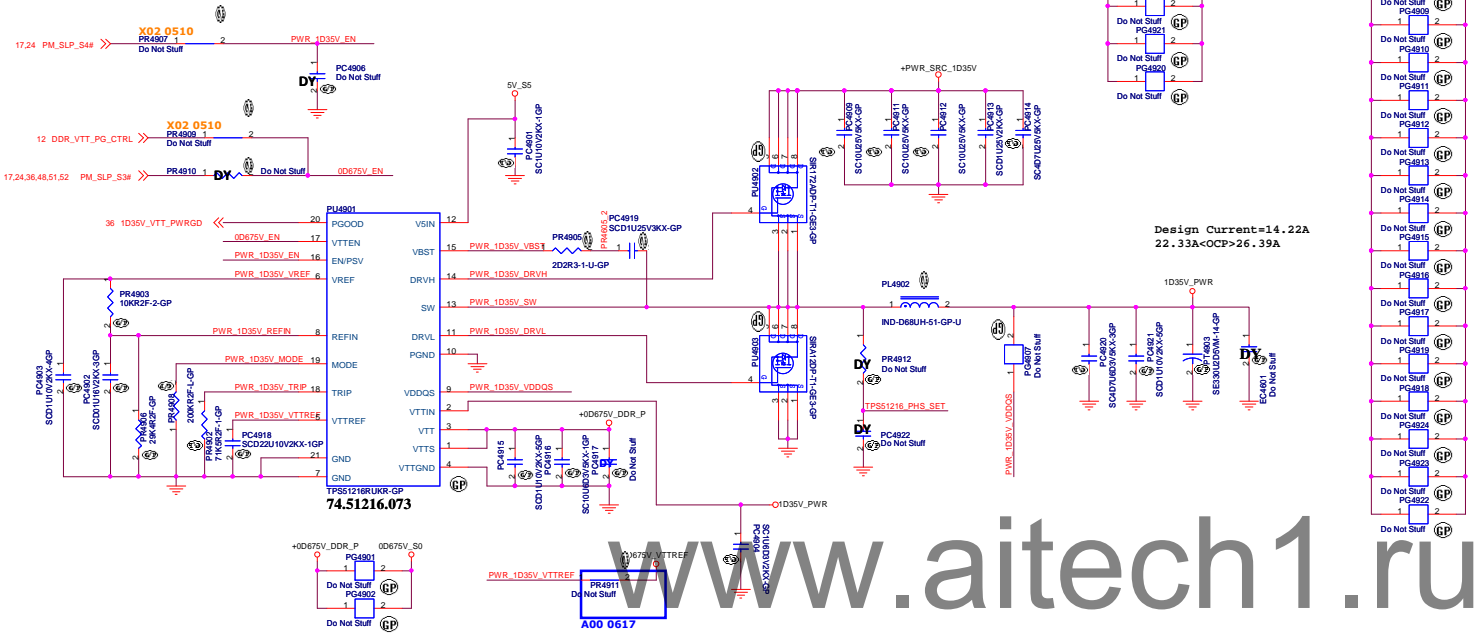
28W CPU need stuff PC4739, PC4724, PC47242, PC4716, PC4741, PC4743

```
SSID = PWR.Plane.Regulator_1p05v
```



I/P cap: CHIP CAP C 100 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5L /78.22610.51L

SSID = PWR.Plane.Regulator 1p35v0p675v



Design Current=14.22A
22.33A<OCP>26.39A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off


MODE		
PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKES 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsui1/77.53371.18L
H/S: S1R172ADP-T1-GE3 / 8.5mohm/10.5mOhm@4.5Vgs/ 84.00172.A37
L/S: S1R12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

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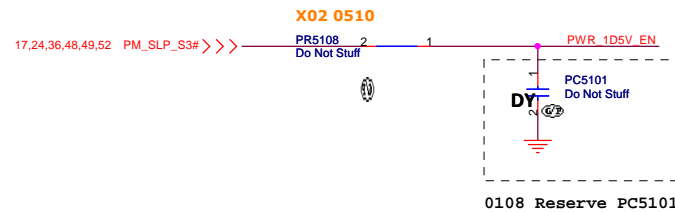
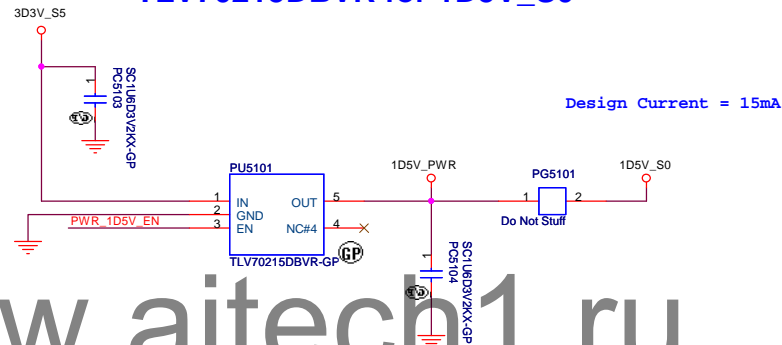
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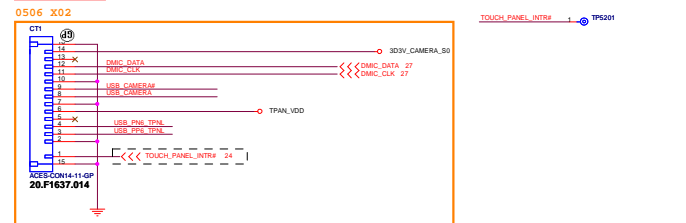
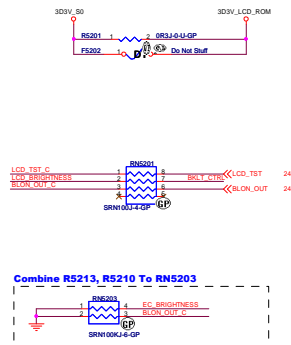
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)TPS51312 1D8V			
Size	Document Number	Rev	
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SSID = PWR.Plane.Regulator_lp5v

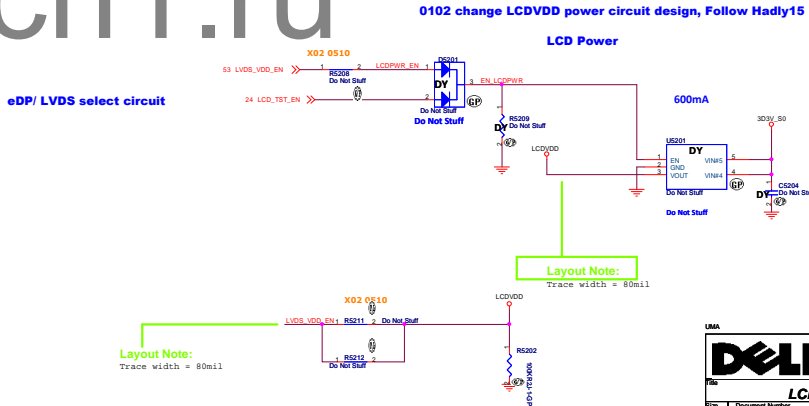
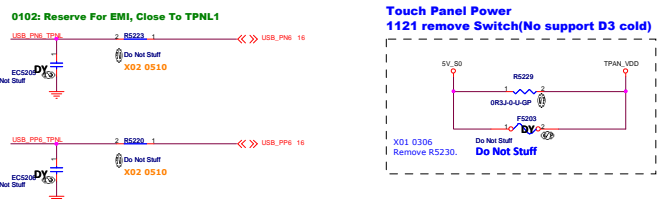
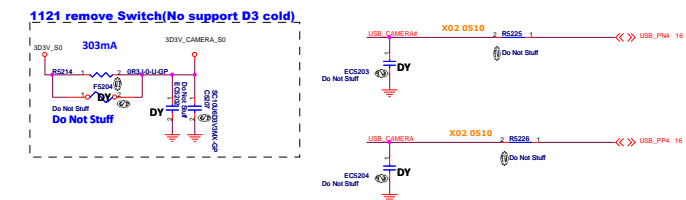
TLV70215DBVR for 1D5V_S0



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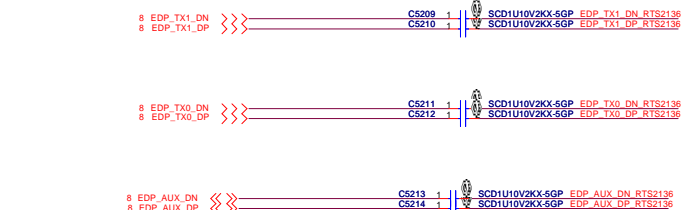
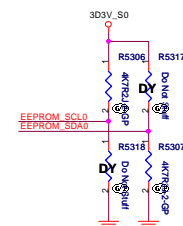
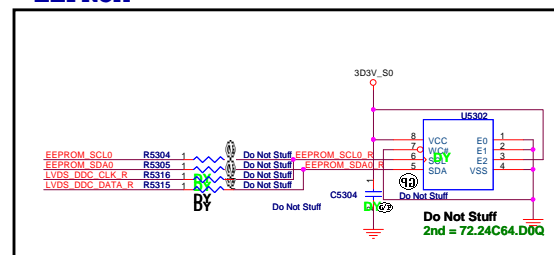
0102: Reserve For EMI, Close To CAM1 Close to LCD connector



LMA	
 <div style="float: right; text-align: right;"> Wistron Corporation 21F, 88, Sec.1, Hsiao Tai Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C. </div>	
File	
LCD Connector Hadley 17"	
Size Custom	Document Number A00
Date January 25, 2013	Page# 55 of 103

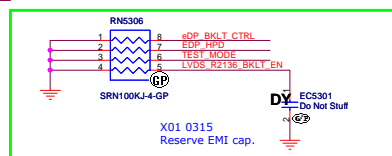
- **Layout Note:**
Place near U5301

EEPROM

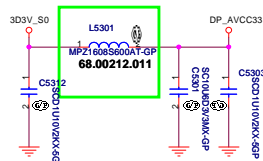


Brightness

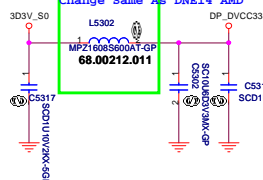
```
0102: Change To 8P4R
0116: SWAP Net
```



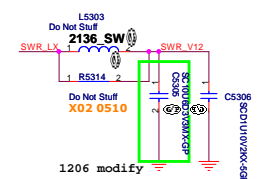
Change Same As DNE14 AMD



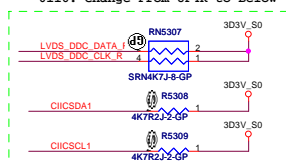
Change Same As DNE14 AMD



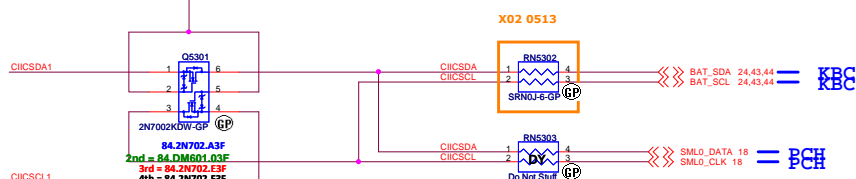
Close to



0116: Change From 8P4R to Below

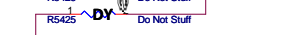
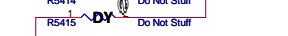
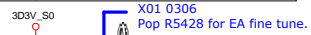


X02 0513

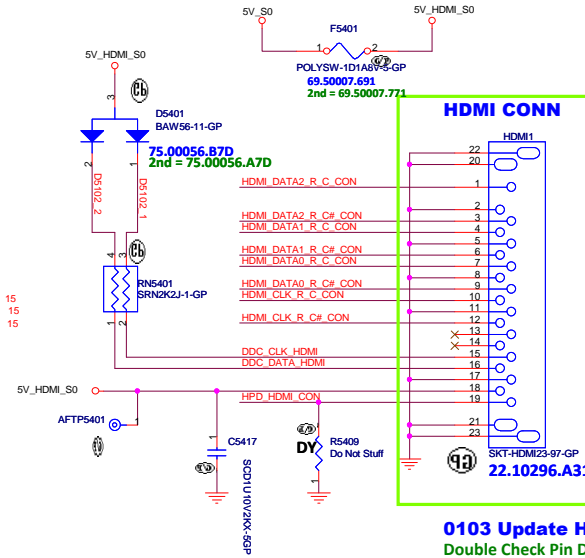
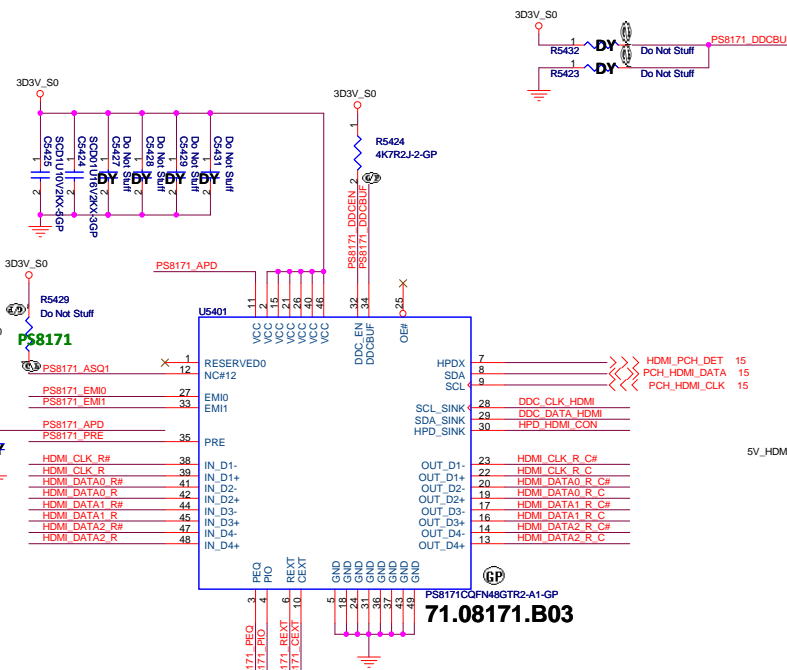
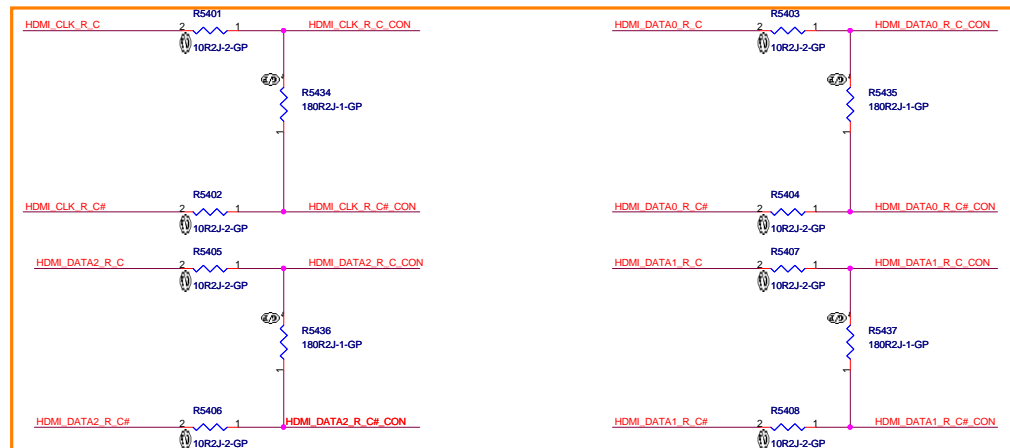


```
2136 Integrated Power Switch
Beware Trace Width If Internal Switch Used.
POP R5322, C5315 R5323 If Used.
POP R5323 DEPOP R5322. C5315 If Used as GPIO for External Switch
```

8	HDMI_CLK#	>>>	C5401	1	SCD1U10V2KX-5GP	HDMI_CLK_# R#
8	HDMI_CLK#	>>>	C5402	1	SCD1U10V2KX-5GP	HDMI_CLK_# R
8	HDMI_DATA0#	>>>	C5403	1	SCD1U10V2KX-5GP	HDMI_DATA0_# R#
8	HDMI_DATA0	>>>	C5404	1	SCD1U10V2KX-5GP	HDMI_DATA0_# R
8	HDMI_DATA1#	>>>	C5405	1	SCD1U10V2KX-5GP	HDMI_DATA1_# R#
8	HDMI_DATA1	>>>	C5406	1	SCD1U10V2KX-5GP	HDMI_DATA1_# R
8	HDMI_DATA2#	>>>	C5407	1	SCD1U10V2KX-5GP	HDMI_DATA2_# R#
8	HDMI_DATA2	>>>	C5408	1	SCD1U10V2KX-5GP	HDMI_DATA2_# R



X02 0515



0103 Update HDMI

Double Check Pin Define

EA fine tune. 

SSID = VIDEO

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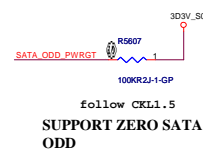
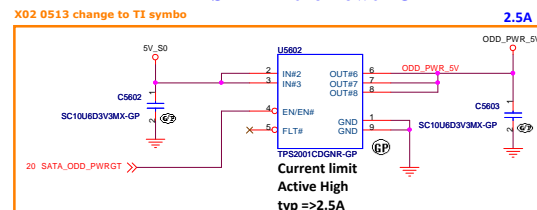
SSID = SATA



EQ1/EQ2	CH1/CH2 Equalization dB (@6Gbps)
NC (default)	0
0	7
1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)


SATA Zero Power ODD



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Title

Size
A3

Document Number
Hadley 17"

Date: Tuesday, June 25, 2013

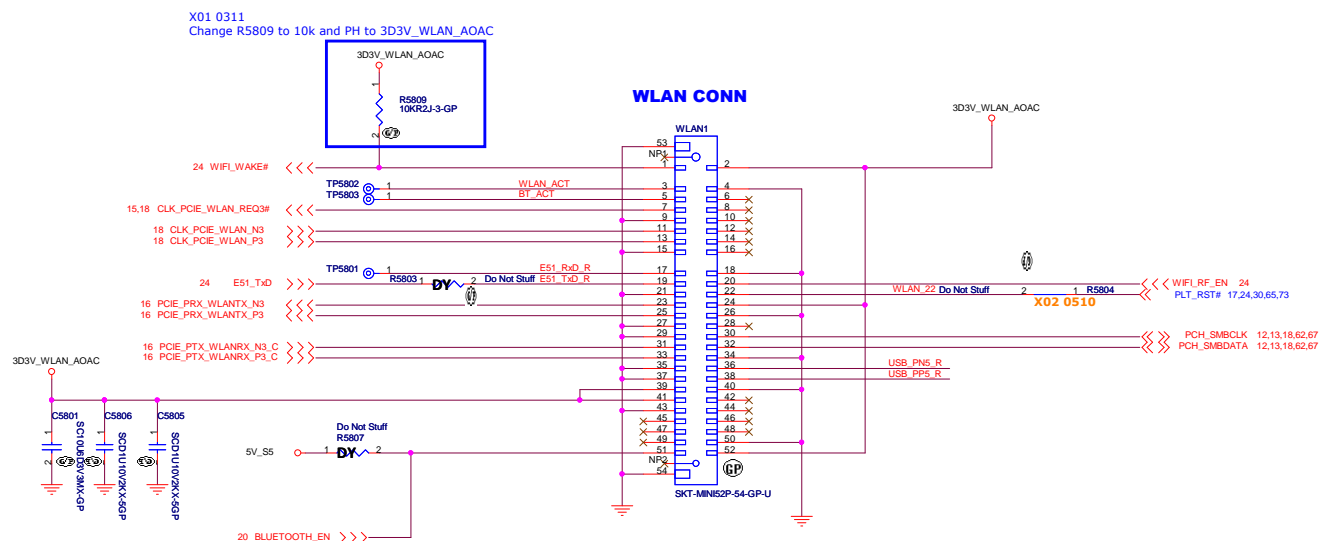
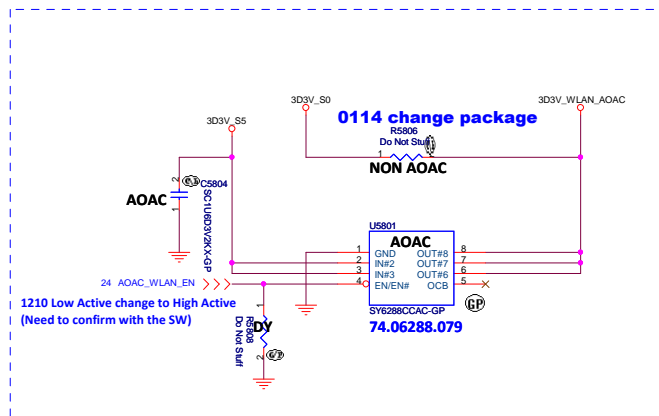
Reserved

Rev
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1

SSID = Wireless



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LIMA



Title			
WLAN/BT			
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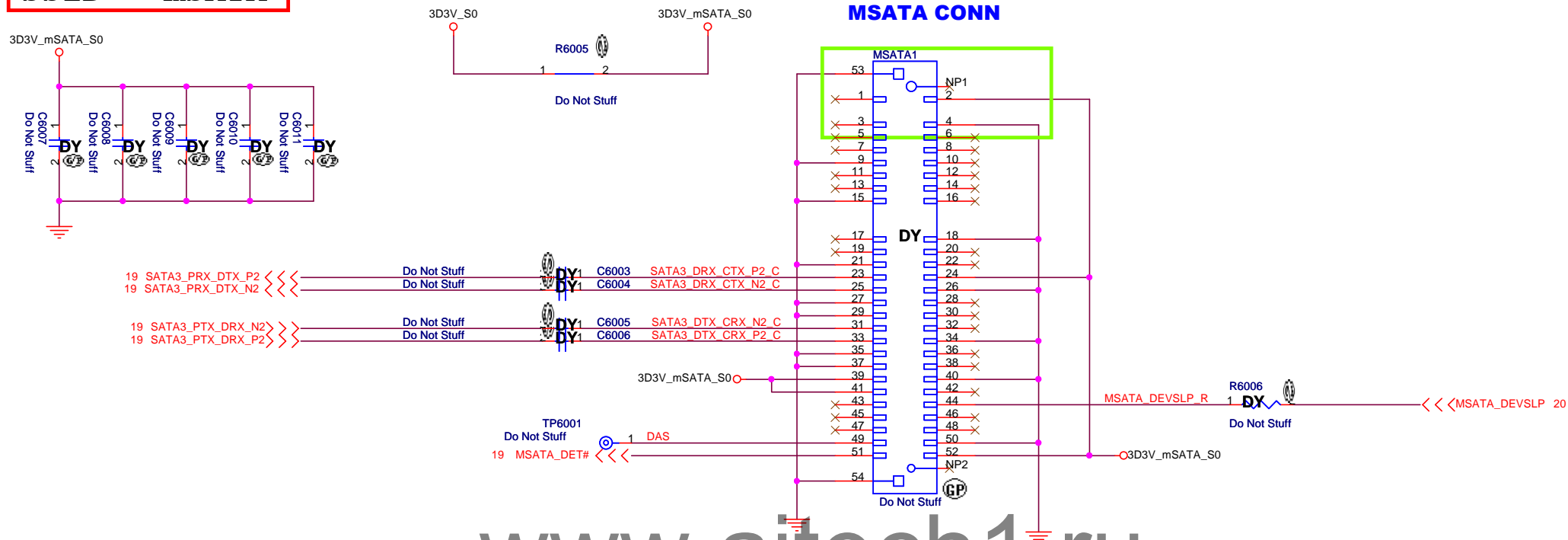
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Title			
Reserved			
Size A4	Document Number Hadley 17"		Rev A00
Date: Tuesday, June 25, 2013		Sheet 59 of	102

SSID = mSATA



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UMA



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Title

mSATA

Size

Document Number

Hadley 17"

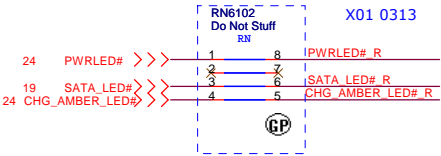
Rev

A00

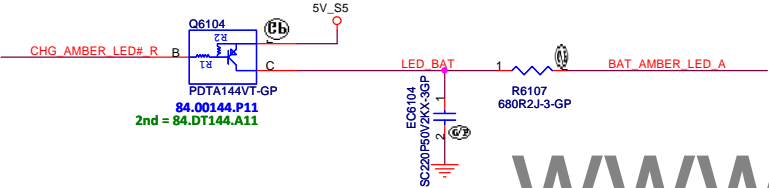
Date: Tuesday, June 25, 2013

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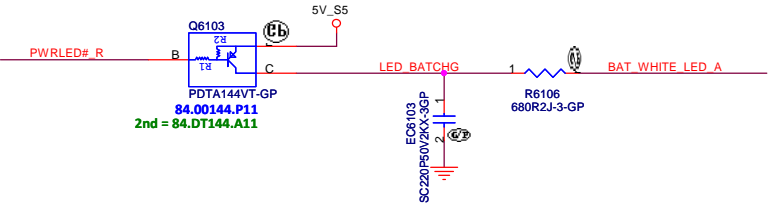
0114 Add



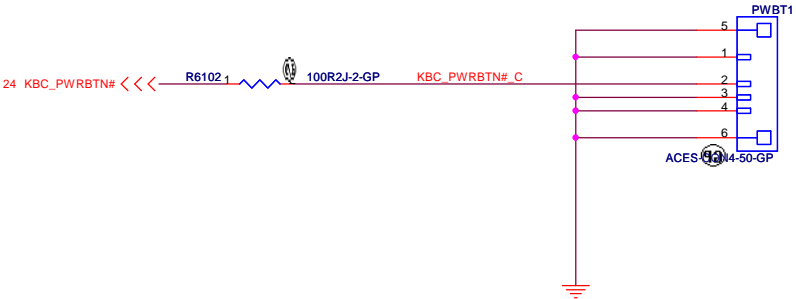
Battery LED1(Amber_LED)
LOW actived from KBC GPIO



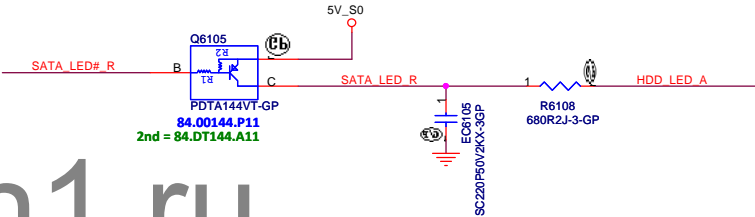
Battery LED2(White_LED)
LOW actived from KBC GPIO



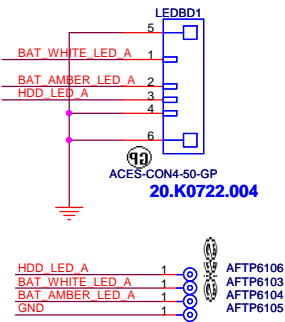
PWRBTN CONN



SATA HDD LED
LOW actived from PCH GPIO

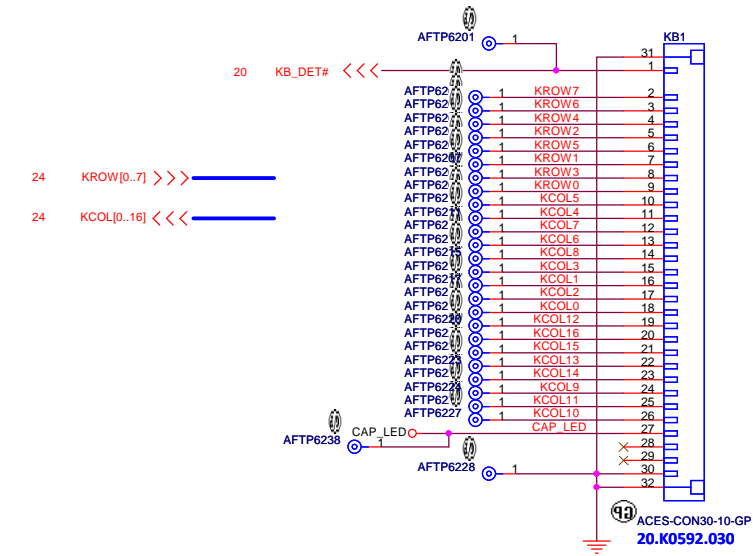


LED board CONN

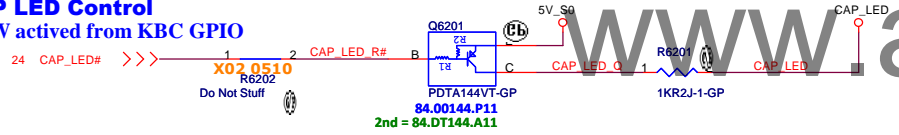


SSID = KBC

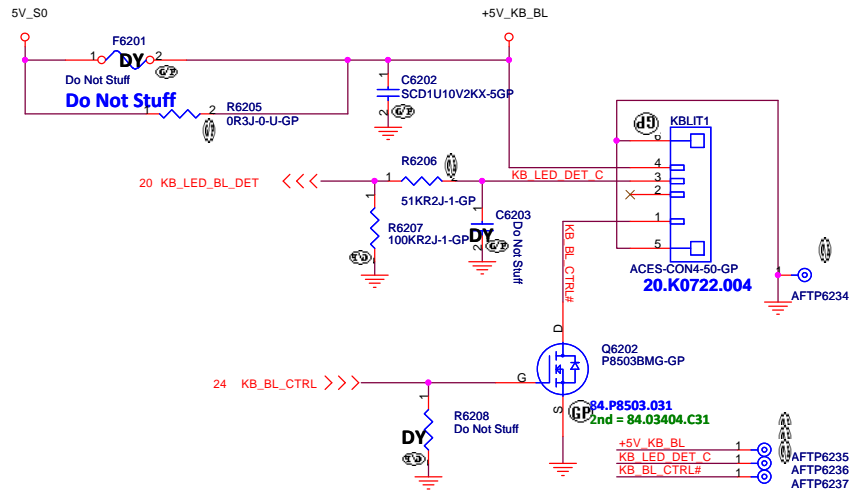
Internal Keyboard Connector



CAP LED Control
LOW acted from KBC GPIO



1109 Add KB backlit

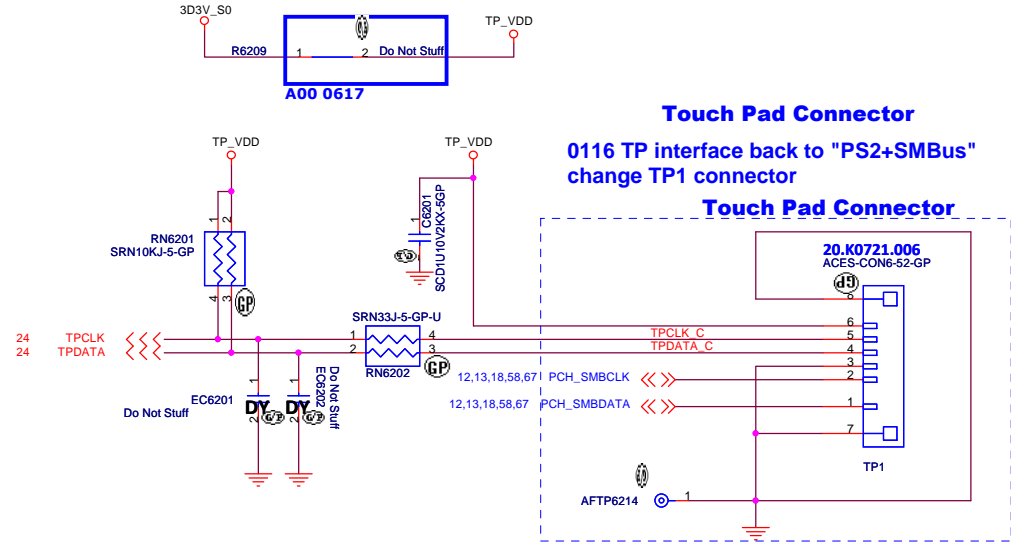


SSID = Touch.Pad

Touch Pad Connector

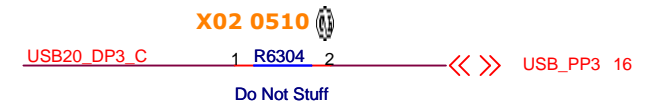
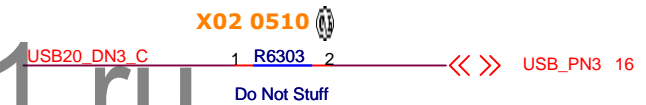
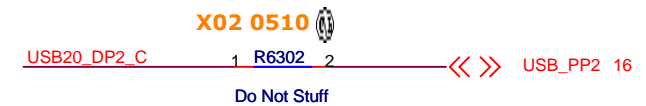
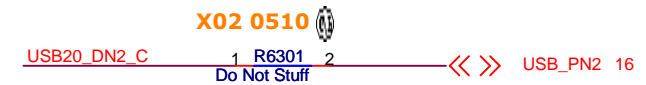
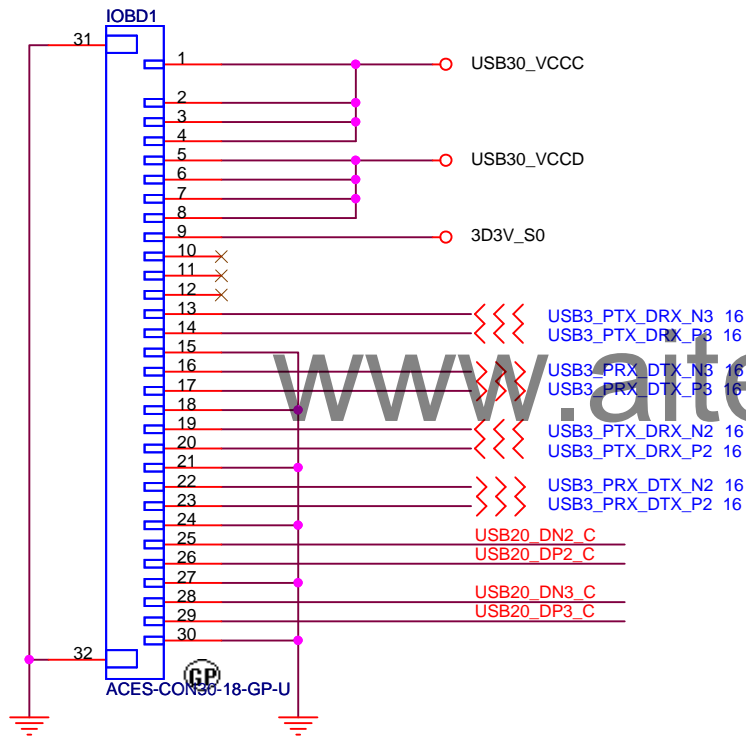
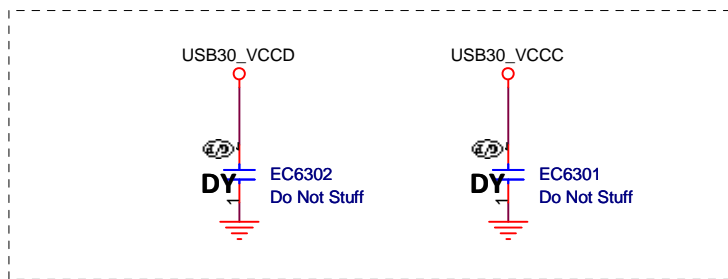
0116 TP interface back to "PS2+SMBus"
change TP1 connector

Touch Pad Connector



Pin number	Pin name
1	VDD
2	TPCLK_C
3	TPDATA_C
4	GND
5	PCH_SMBCLK
6	PCH_SMBDATA

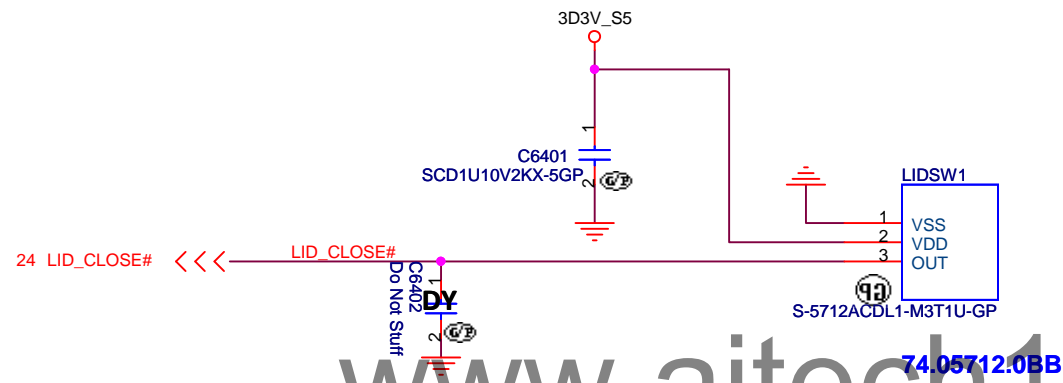
SSID = User.Interface



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DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title IO Board Connector			
Size A4	Document Number Hadley 17"		Rev A00
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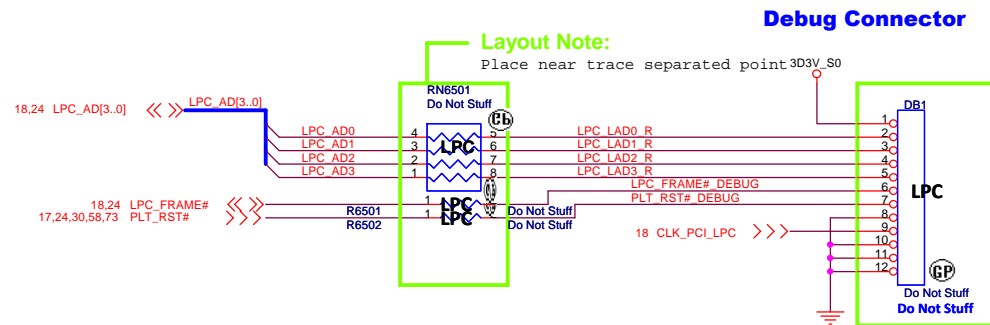
SSID = User.Interface



UMA

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Hall Sensor			
Size A4	Document Number Hadley 17"		Rev A00
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SSID = DEBUG PORT



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(Blanking)

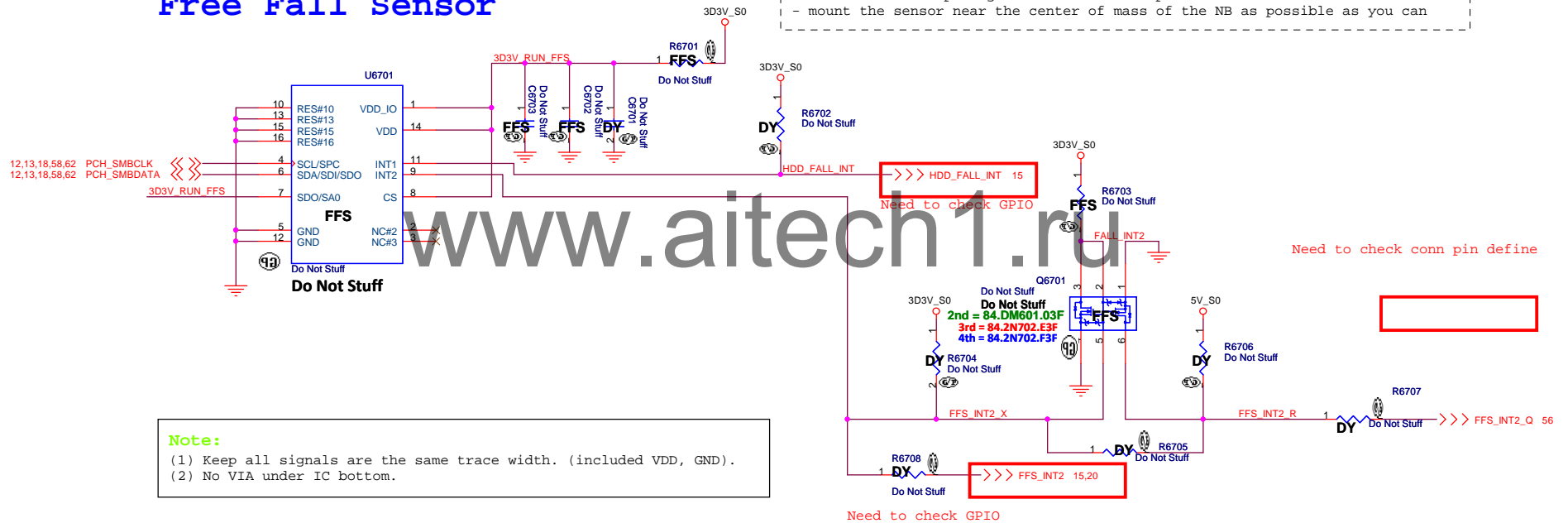
UMA

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Title Reserved			
Size A4	Document Number Hadley 17"		Rev A00
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Free Fall Sensor

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can




Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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Title

Size
A3

Document Number
Hadley 17"

Rev
A00

Date: Tuesday, June 25, 2013

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Title

Reserved

Size
A

Document Number

Hadley 17"

Rev

A00

Date: Tuesday, June 25, 2013

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Title

Reserved

Size
A

Document Number

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Rev

A00

Date: Tuesday, June 25, 2013

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Title

Reserved

Size
A

Document Number

Hadley 17"

Rev

A00

Date: Tuesday, June 25, 2013

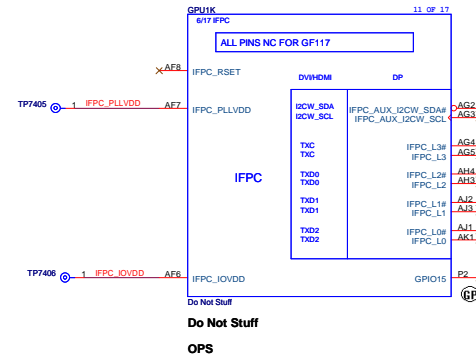
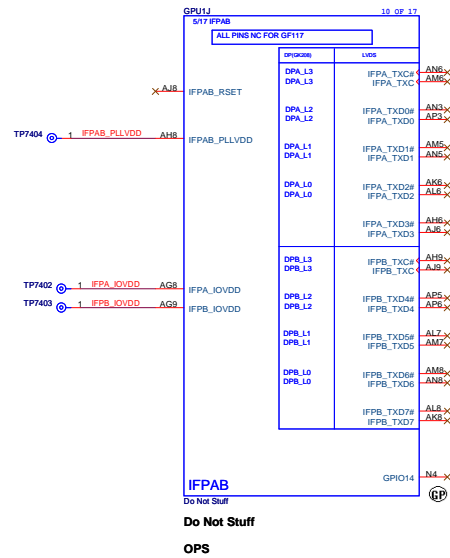
Sheet 71 of 102

(Blanking)
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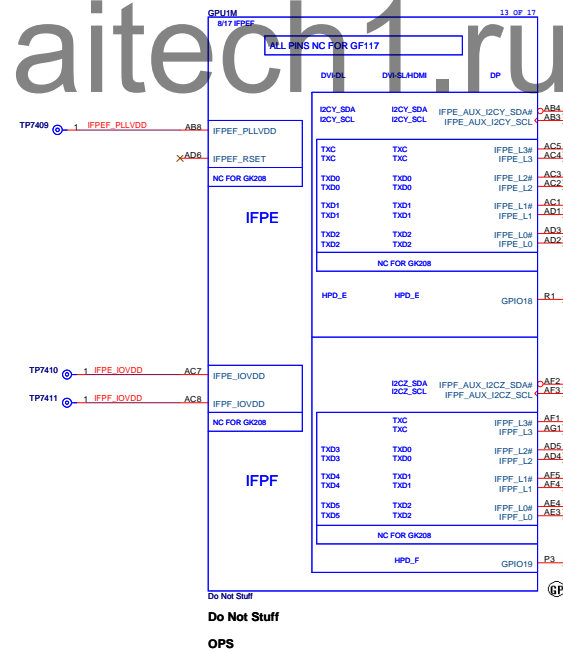
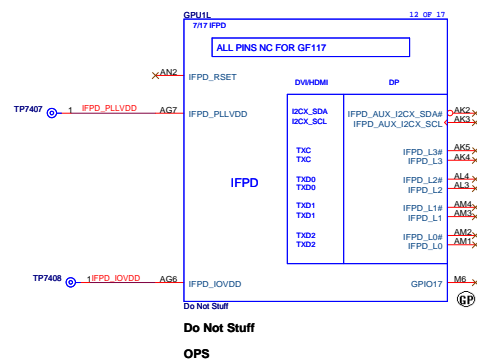
UMA

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Title			
Reserved			
Size A4	Document Number Hadley 17"		Rev A00
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LVDS Interface



HDMI Interface





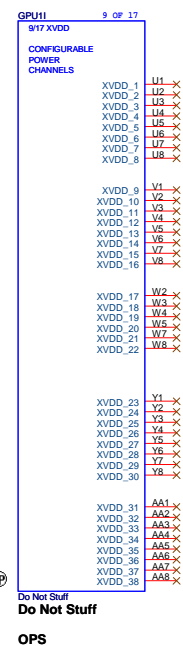
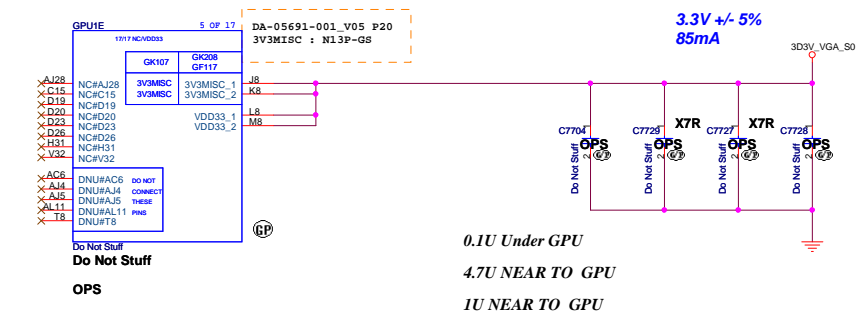
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V/ 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production ready
		0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4G20325FD-FC04	2500	1219	Production ready
		0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate


Table 121. Resistance Mapping to Hex Values

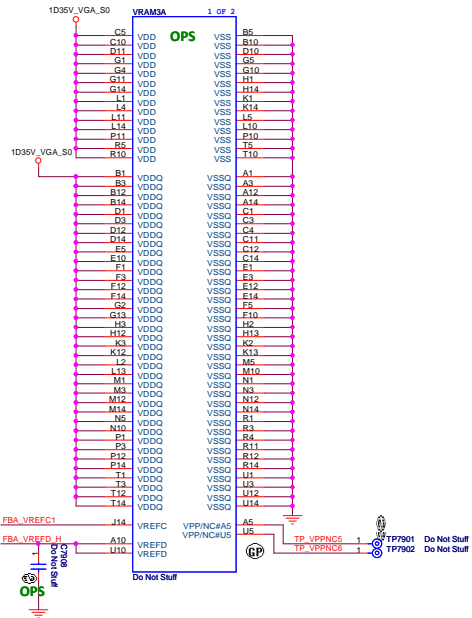
Strain ID Name	Logarithmic screening (SIR)	Logarithmic screening (SIR)	Logarithmic screening (SIR)	Logarithmic screening (SIR)	
NON-SIR	PCG_VIR001	SIR_VERSION	PCG_VIR003	PCG_P1_1.W_VIR.W	
NON-SIR	RANCQ_021	RANCQ_022	RANCQ_023	RANCQ_020	
NON-SIR	1	1	1	1	
STRAP1	0000000	0000000	0000000	0000000	Not strain path-1
STRAP2	0000000	0000000	0000000	0000000	
STRAP3	0000000	0000000	0000000	0000000	Not strain path-2
STRAP4	0000000	0000000	0000000	0000000	
STRAP5	0000000	0000000	0000000	0000000	Not strain path-3
STRAP6	0000000	0000000	0000000	0000000	
STRAP7	0000000	0000000	0000000	0000000	Not strain path-4
STRAP8	0000000	0000000	0000000	0000000	
STRAP9	0000000	0000000	0000000	0000000	Not strain path-5
STRAP10	0000000	0000000	0000000	0000000	
STRAP11	0000000	0000000	0000000	0000000	Not strain path-6
STRAP12	0000000	0000000	0000000	0000000	
STRAP13	0000000	0000000	0000000	0000000	Not strain path-7
STRAP14	0000000	0000000	0000000	0000000	
STRAP15	0000000	0000000	0000000	0000000	Not strain path-8
STRAP16	0000000	0000000	0000000	0000000	
STRAP17	0000000	0000000	0000000	0000000	Not strain path-9
STRAP18	0000000	0000000	0000000	0000000	
STRAP19	0000000	0000000	0000000	0000000	Not strain path-10
STRAP20	0000000	0000000	0000000	0000000	
STRAP21	0000000	0000000	0000000	0000000	Not strain path-11
STRAP22	0000000	0000000	0000000	0000000	
STRAP23	0000000	0000000	0000000	0000000	Not strain path-12
STRAP24	0000000	0000000	0000000	0000000	
STRAP25	0000000	0000000	0000000	0000000	Not strain path-13
STRAP26	0000000	0000000	0000000	0000000	
STRAP27	0000000	0000000	0000000	0000000	Not strain path-14
STRAP28	0000000	0000000	0000000	0000000	
STRAP29	0000000	0000000	0000000	0000000	Not strain path-15
STRAP30	0000000	0000000	0000000	0000000	
STRAP31	0000000	0000000	0000000	0000000	Not strain path-16
STRAP32	0000000	0000000	0000000	0000000	
STRAP33	0000000	0000000	0000000	0000000	Not strain path-17
STRAP34	0000000	0000000	0000000	0000000	
STRAP35	0000000	0000000	0000000	0000000	Not strain path-18
STRAP36	0000000	0000000	0000000	0000000	
STRAP37	0000000	0000000	0000000	0000000	Not strain path-19
STRAP38	0000000	0000000	0000000	0000000	
STRAP39	0000000	0000000	0000000	0000000	Not strain path-20
STRAP40	0000000	0000000	0000000	0000000	
STRAP41	0000000	0000000	0000000	0000000	Not strain path-21
STRAP42	0000000	0000000	0000000	0000000	
STRAP43	0000000	0000000	0000000	0000000	Not strain path-22
STRAP44	0000000	0000000	0000000	0000000	
STRAP45	0000000	0000000	0000000	0000000	Not strain path-23
STRAP46	0000000	0000000	0000000	0000000	
STRAP47	0000000	0000000	0000000	0000000	Not strain path-24
STRAP48	0000000	0000000	0000000	0000000	
STRAP49	0000000	0000000	0000000	0000000	Not strain path-25
STRAP50	0000000	0000000	0000000	0000000	
STRAP51	0000000	0000000	0000000	0000000	Not strain path-26
STRAP52	0000000	0000000	0000000	0000000	
STRAP53	0000000	0000000	0000000	0000000	Not strain path-27
STRAP54	0000000	0000000	0000000	0000000	
STRAP55	0000000	0000000	0000000	0000000	Not strain path-28
STRAP56	0000000	0000000	0000000	0000000	
STRAP57	0000000	0000000	0000000	0000000	Not strain path-29
STRAP58	0000000	0000000	0000000	0000000	
STRAP59	0000000	0000000	0000000	0000000	Not strain path-30
STRAP60	0000000	0000000	0000000	0000000	
STRAP61	0000000	0000000	0000000	0000000	Not strain path-31
STRAP62	0000000	0000000	0000000	0000000	
STRAP63	0000000	0000000	0000000	0000000	Not strain path-32
STRAP64	0000000	0000000	0000000	0000000	
STRAP65	0000000	0000000	0000000	0000000	Not strain path-33
STRAP66	0000000	0000000	0000000	0000000	
STRAP67	0000000	0000000	0000000	0000000	Not strain path-34
STRAP68	0000000	0000000	0000000	0000000	
STRAP69	0000000	0000000	0000000	0000000	Not strain path-35
STRAP70	0000000	0000000	0000000	0000000	
STRAP71	0000000	0000000	0000000	0000000	Not strain path-36
STRAP72	0000000	0000000	0000000	0000000	
STRAP73	0000000	0000000	0000000	0000000	Not strain path-37
STRAP74	0000000	0000000	0000000	0000000	
STRAP75	0000000	0000000	0000000	0000000	Not strain path-38
STRAP76	0000000	0000000	0000000	0000000	
STRAP77	0000000	0000000	0000000	0000000	Not strain path-39
STRAP78	0000000	0000000	0000000	0000000	
STRAP79	0000000	0000000	0000000	0000000	Not strain path-40
STRAP80	0000000	0000000	0000000	0000000	
STRAP81	0000000	0000000	0000000	0000000	Not strain path-41
STRAP82	0000000	0000000	0000000	0000000	
STRAP83	0000000	0000000	0000000	0000000	Not strain path-42
STRAP84	0000000	0000000	0000000	0000000	
STRAP85	0000000	0000000	0000000	0000000	Not strain path-43
STRAP86	0000000	0000000	0000000	0000000	
STRAP87	0000000	0000000	0000000	0000000	Not strain path-44
STRAP88	0000000	0000000	0000000	0000000	
STRAP89	0000000	0000000	0000000	0000000	Not strain path-45
STRAP90	0000000	0000000	0000000	0000000	
STRAP91	0000000	0000000	0000000	0000000	Not strain path-46
STRAP92	0000000	0000000	0000000	0000000	
STRAP93	0000000	0000000	0000000	0000000	Not strain path-47
STRAP94	0000000	0000000	0000000	0000000	
STRAP95	0000000	0000000	0000000	0000000	Not strain path-48
STRAP96	0000000	0000000	0000000	0000000	
STRAP97	0000000	0000000	0000000	0000000	Not strain path-49
STRAP98	0000000	0000000	0000000	0000000	
STRAP99	0000000	0000000	0000000	0000000	Not strain path-50
STRAP100	0000000	0000000	0000000	0000000	

DATE	TIME	FROM	TO	STATUS	REMARKS
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2019-01-01	00:00	00:00	00:00	00:00	00:00

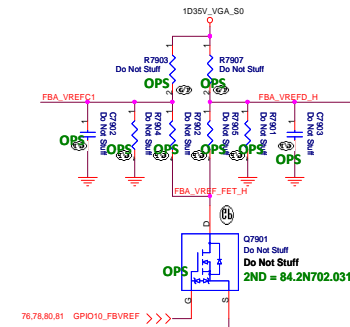
Under GPU



UMA				
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Title				
GPU POWER(4/5)				
Size	Document Number			Rev
Custom	Hadley 17"			A00
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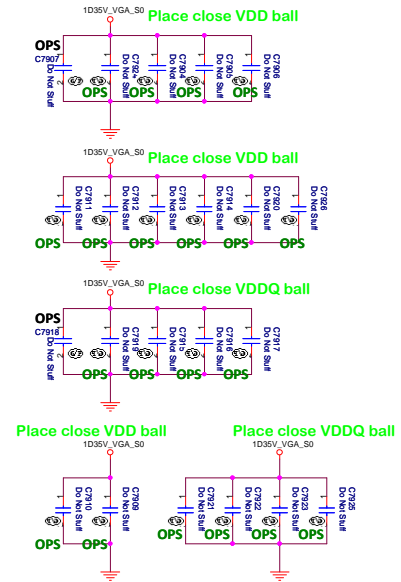
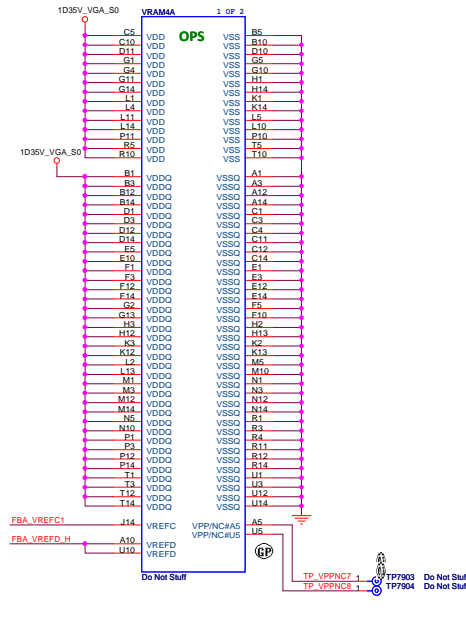
Frame Buffer Partition A-Upper Half



FBVREF Termination

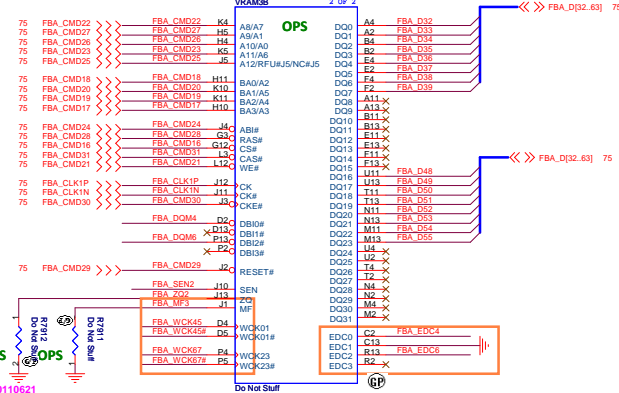
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

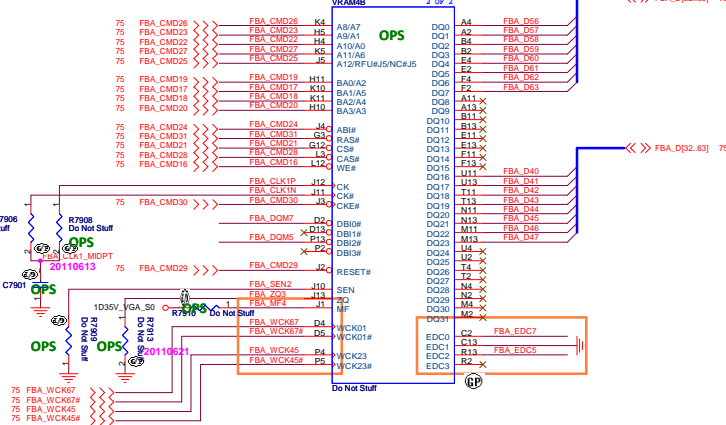


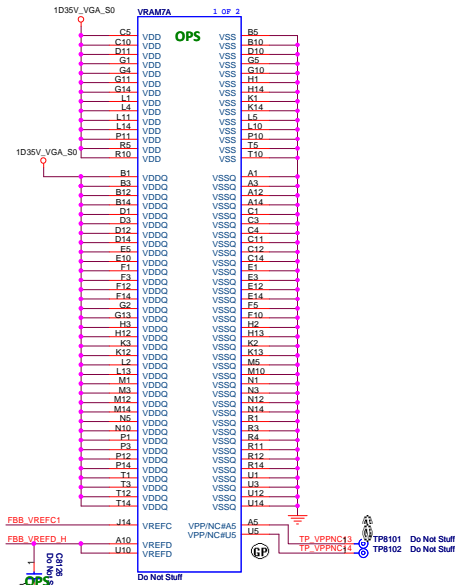
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Normal(MF=0)

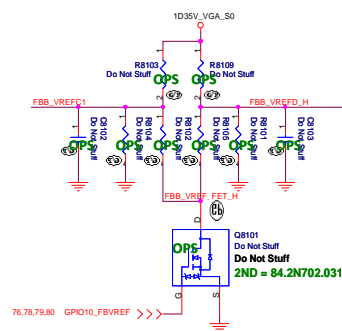


Mirrored(MF=1)





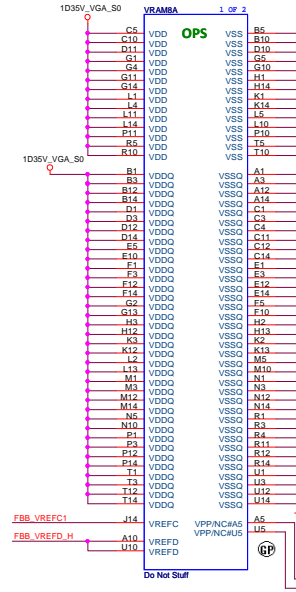
Frame Buffer Partition B-Upper Half



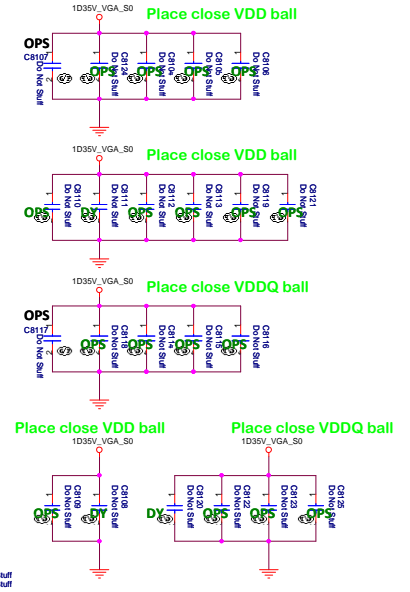
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

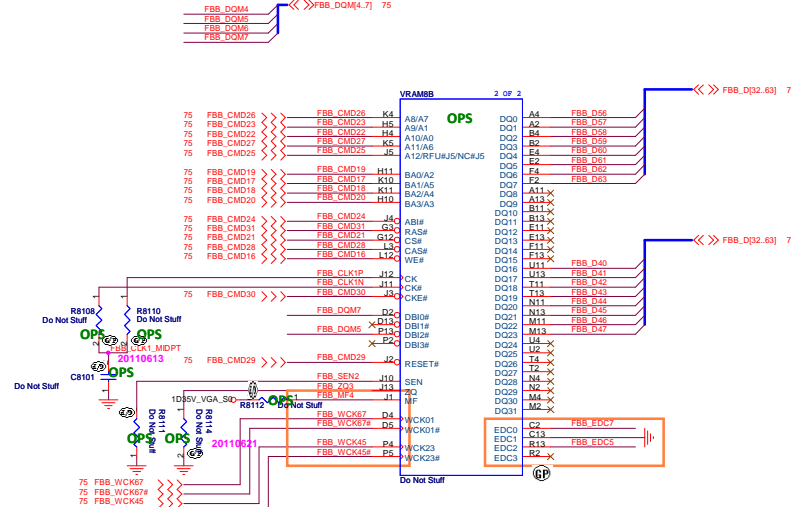
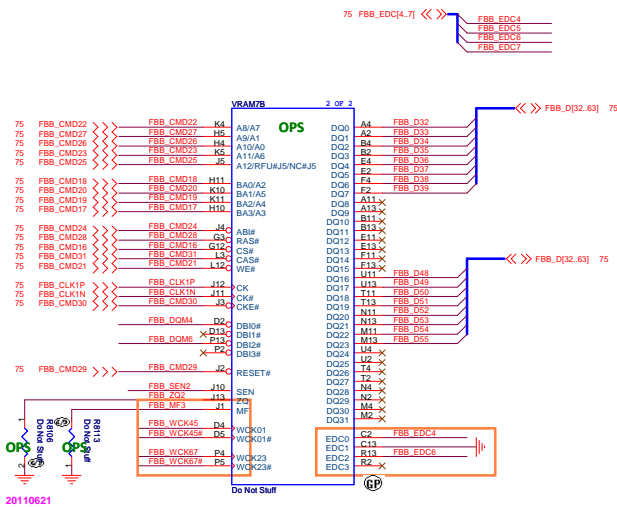


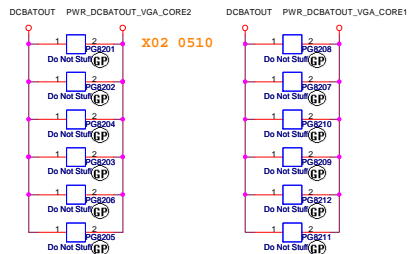
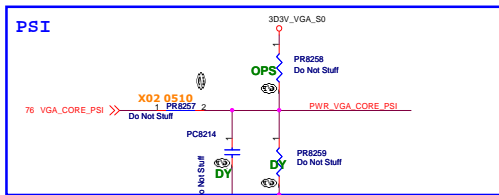
Mirrored(MF=1)



Normal(MF=0)

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PWR_VGA_CORE1

PUI8202

OPS

PUI8208

OPS

PC8220

PC8221

PC8222

PC8223

PC8227

Do Not Stuff

PWR_VGA_CORE_H01

PWR_VGA_CORE_SW1

PWR_VGA_CORE_L01

CYNTec

D22uH/DCR=1mohm (max)

PL8201

Do Not Stuff

OPS

PUI8203

OPS

PUI8204

OPS

PT8210

OPS

PT8211

OPS

VGA_CORE

PWR_VGA_CORE_H02

PWR_VGA_CORE_SW2

PWR_VGA_CORE_L02

The schematic diagram illustrates the power and signal connections for the PWR_VGA_CORE section of the Xilinx Zynq-7010. Key components and connections include:

- Power Supply:** 5V_55 supply connected to the PWR_VGA_CORE_VCC pin (21) of the PWR_VGA_CORE block.
- Grounding:** 81172_AGN2 pin connected to the GND pin (25) of the PWR_VGA_CORE block.
- Signal Connections:**
 - PWR_VGA_CORE_EN (3) connected to EN pin (3) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_PSI (4) connected to PSI pin (4) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_TALERTA (5) connected to TALERTA pin (5) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_VBD (6) connected to VBD pin (6) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_TSENSE (13) connected to TSENSE pin (13) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_VREF (8) connected to VREF pin (8) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_VDBUF (9) connected to VDBUF pin (9) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_FB (12) connected to FB pin (12) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_FBTN (17) connected to FBTN pin (17) of the PWR_VGA_CORE block.
 - PWR_VGA_CORE_COMP (18) connected to COMP pin (18) of the PWR_VGA_CORE block.
- Resistors:** R1, R2, R3, R4, R5 are connected to the PWR_VGA_CORE_VBD pin (6).
- Capacitors:** C1, C2 are connected to the PWR_VGA_CORE_VCC pin (21).
- Logic Gates:** PR8201, PR8202, PR8203, PR8204, PR8205, PR8206, PR8207, PR8208, PR8209, PR8210, PR8211, PR8212, PR8213, PR8214, PR8215, PR8216, PR8217, PR8218, PR8219, PR8220, PR8221, PR8222, PR8223, PR8224, PR8225, PR8226, PR8227, PR8228, PR8229 are connected to the PWR_VGA_CORE_VCC pin (21).
- Annotations:**
 - "Do Not Stuff" is written next to many components.
 - "X02 0510" is written next to the PWR_VGA_CORE_VBD pin (6).
 - "N14P-GT is ConfigB" and "N14E-GL is ConfigB" are written in a pink box.

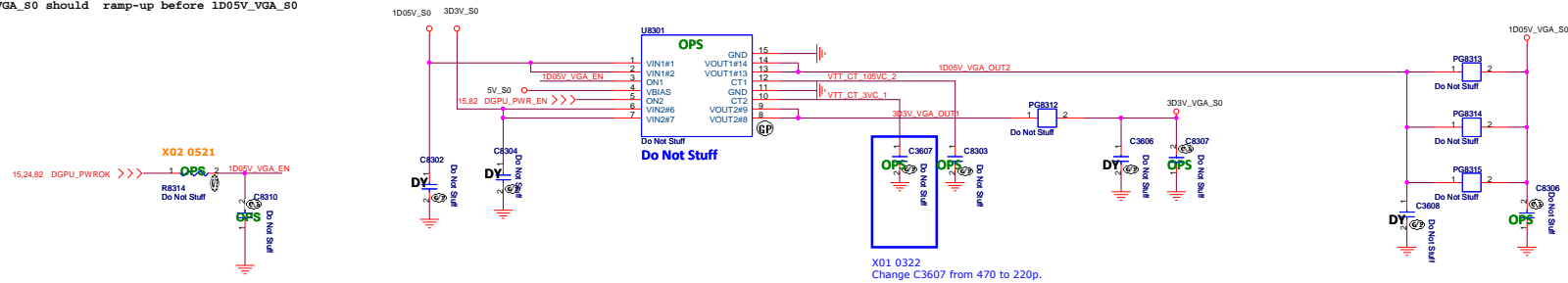
VGA type	Config	Design Current	EDP-peak	OCF	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCP<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCP<78A	20K	20K	2K	18K	0	2.7nF
N14P-GT	B	45A	75A	82.5A<OCP<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCP<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCP<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCP<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCP<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCP<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCP<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCP<93.98A	20K	20K	2K	18K	0	2.7nF

PWM-VID Spec		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width $T_{D(Off)}$	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	K Ω	39	20	39
R2 (1%)	K Ω	39	20	30
R3 (1%)	K Ω	1.5	2	3
R4 (1%)	K Ω	30	18	24
R5 (1%)	K Ω	1.5	0	3
C	nF	1.5	2.7	1.8

1D05V_VGA_S0

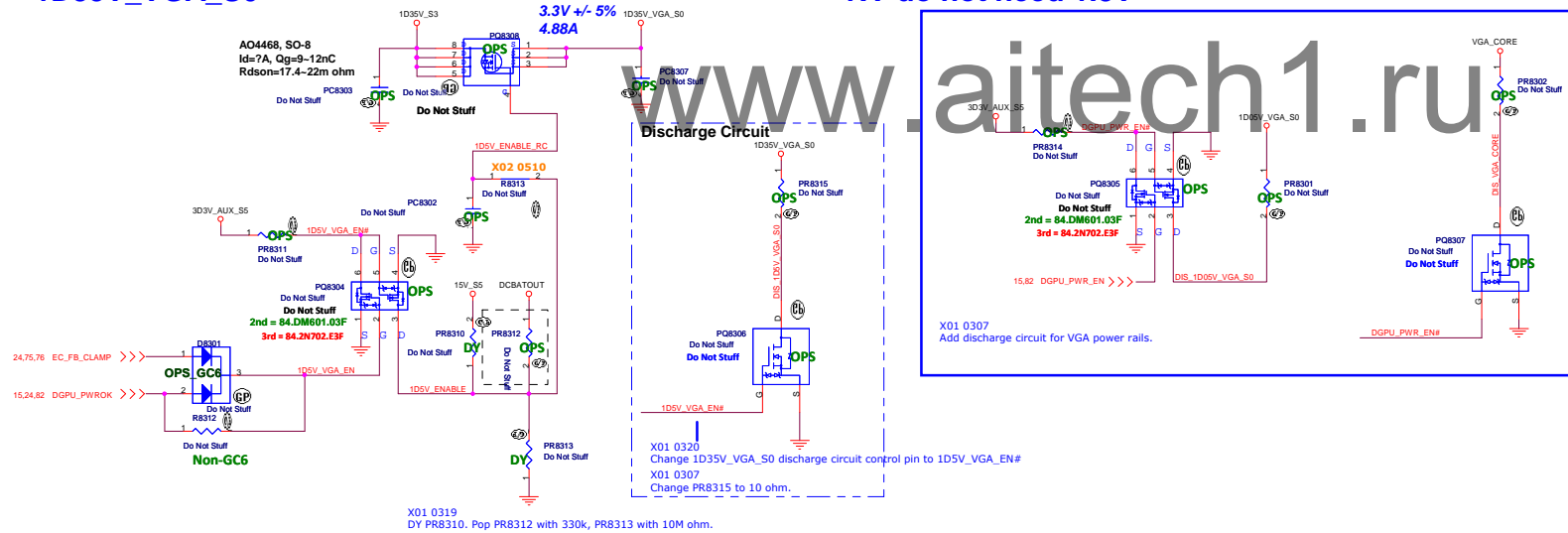
```
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp-up before 1D05V_VGA_S0
```

```
3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0
```



1D35V_VGA_S0


NV do not need 1.8V



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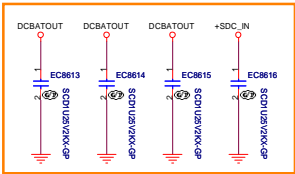
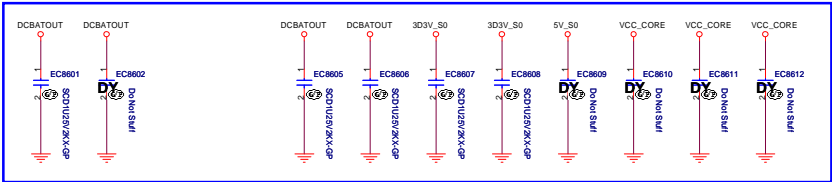
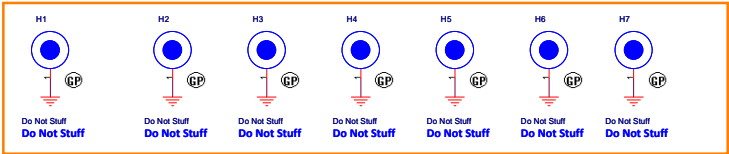
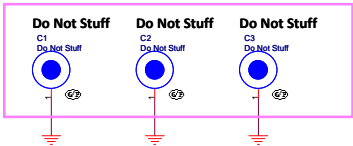
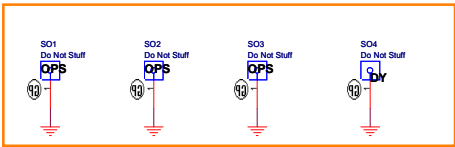
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SSID = User.Interface




X02 0510

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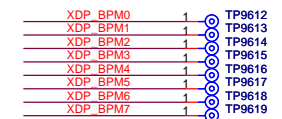
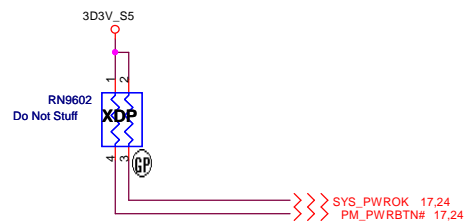
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SSID = XDP

CPU XDP



UMA

X01 0227 P.24 Change R2404 to 20k for PCB version.
0306 P.52 Remove R5230. DY F5203.
P.54 Change R5410 from 499 to 487 ohm for EA fine tune.
P.54 Pop R5428 for EA fine tune.
0307 P.82 DY PR8263, pop PR8265 with 1.8k for sequence.
P.83 Change PR8315 to 10 ohm.
P.83 Add discharge circuit for VGA power rails.
0311 P.25 Remove SKT25.
P.29 Change HPMIC1 from 22.10270.S81 to 22.10270.V01
P.33 Change CARD1 from 62.10051.C61 to 62.10051.H21
P.34 Change USB1 from 22.10341.691 to 22.10339.W31
P.43 Change BATT1 from 20.81646.008 to 20.82046.008
P.17 Remove OBFF circuit.
P.17 Change R1705 to 1k and PH to 3D3V_S5
P.30 Remove R3024. Change R3039 to 10k and PH to 3D3V_LAN_S5
P.58 Change R5809 to 10k and PH to 3D3V_LAN_S5
P.20 Add TP2004 and change net name to MCP_GPIO16.
0312 P.63 Re-arrange IOBD1 pin1~pin12.
0313 Change R404 R711 R1101 R1102 R1104 R1105 R1201
R1202 R1302 R1801 R1807 R1808 R1809 R1811 R1812
R1904 R2101 R2103 R2105 R2112 R2117 R2118 R2401
R2402 R2408 R2409 R2410 R2419 R2420 R2422 R2427
R2428 R2430 R2435 R6005 RN1806 RN6102 to 0 ohm short pad.
P.24 Change R2447 to D2402 for leakage issue.
0314 P.18 Change CLKREQ port
PCIE port3 use req2
PCIE port4 use req3
PCIE port5 use req4
0315 Reserve EMI cap, EC5207 EC5208 EC5301 EC8601~EC8612.
0318 P.21 Change U2101 from 74.22965.093 to 74.59147.093 for sequence concern. And remove C2140.
P.86 Remove EC8603 EC8604.
P.44 1. Dummy PR4459.
2. Stuff PR4458.
3. Add PC4433.
4. Dummy PR4452, PR4454, PRPR4464.
5. Dummy PC4409, PC4431.
6. Dummy PQ4412.
7. PR4436 change to 220K.
8. PR4442 change to 412K.
9. Dummy PR4441, PR4440, PR4442, PR4447.
P.45 1. Dummy PC4525, PC4526, PC4532, PC4533, PC4534, PC4527.
2. PD4502, PD4503.
0319 P.18 Change CL cap C1801 C1802 to 15p based on vendor test result.
P.30 Change CL cap C3001 C3011 to 15p based on vendor test result.
P.76 Change CL cap C7607 C7608 to 15p based on vendor test result.
P.83 DY PR8310. Pop PR8312 with 330k, PR8313 with 10M ohm.
0320 P.35 Modify USB charger circiut.
P.83 Change 1D35V_VGA_S0 discharge circuit control pin to 1D5V_VGA_EN#
P.18 Change CLKOUT port mapping with REQ port
PCIE port3 use CLK2
PCIE port4 use CLK3
PCIE port5 use CLK4
0321 P.20 Change short pad to 0 ohm for power breakdown.
R2001 R2002 R2004 R2007 R2015 R2016 R2017 R2019 R2020 R2021 R2022 R2023.
P.35 Add R3507 for debug.
P.42 Change EL4201 EL4202 to shortpad and add EL4203.
0322 P.44 Change PG4403 PG4404 PG4405 PG4407 to ZZ.CLOSE.001
P.44 DY PU4407, POP PU4408.
P.82 Change PR8216 to 6.98k ohm.
P.82 Change PR8265 to 12k for sequence.
P.83 Change C3607 from 470 to 220p.

0325 P.46,47 1. PR4609 change to 75K.
2. PR4610 change to 422K.
3. PR4620 change to 3K.
4. PR4704 change to 2.21K.
5. PR4706 change to 2.94K
6. PR4705 change to 29.4K.
7. Stuff PR4701.
8. Stuff PC4701 and change 820P.
9. Stuff PC4715, PC4740.
0326 P.35 Change U3501 to 74.55583.A73
P.44 PR4402 change to 316K.
PR4401 change to 357K.
PR4420 change to 147K.
X02 0502 P.19 change C1903,C1904 from 18pF to 15pF by 32.768khz X'tal (vendor suggested)
P.52 modify BKLt_CTRL circuit; D5202 dual diode change to single diode, R5222 stuff by AUO panel issue
P.52 Modify LED BACKLIGHT CONVERTER POWER for DC mode S5 leakage
0506 P.52 To combine Camera and Touch panel connector
0508 P.21 add C2103 0.47uF for VccDSW3_3 and DcpSusByp to address temporary inrush currents.
0510 P. Change 0 ohm to short pad
Add EMC capacity for DCBATOUT/PS_ID_R/+SDC_IN
Change EL4201~EL4203 to bead
0513 P.53 Change RN1702 and RN5302 to 0ohm
0513 P.56 Change U5602 symbol to TI for BOM
0513 P.56 Change power schematic
1. Add PC4434 (10uF 25V).
2. PD4405 change to short Pad (ZZ.00PAD.5B1).
3. PC4607 change to 78.10610.5FL.
0513 P.56 Remove R1810 short pad,change HDMI brige R5434~R5437 180 ohm and R5401~R5408 to 10 ohm
A00 0618 P. change 0ohm to short pad
0618 P.27 Change R2716 to L2701
0619 P.7 Reserve TI solution to fix C10 issue.

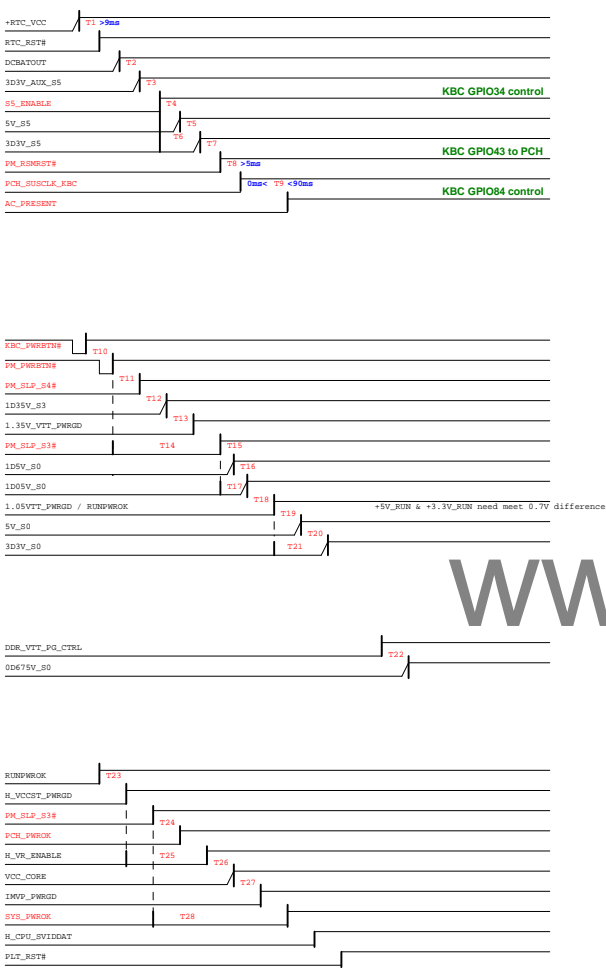
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Intel-Power Up Sequence

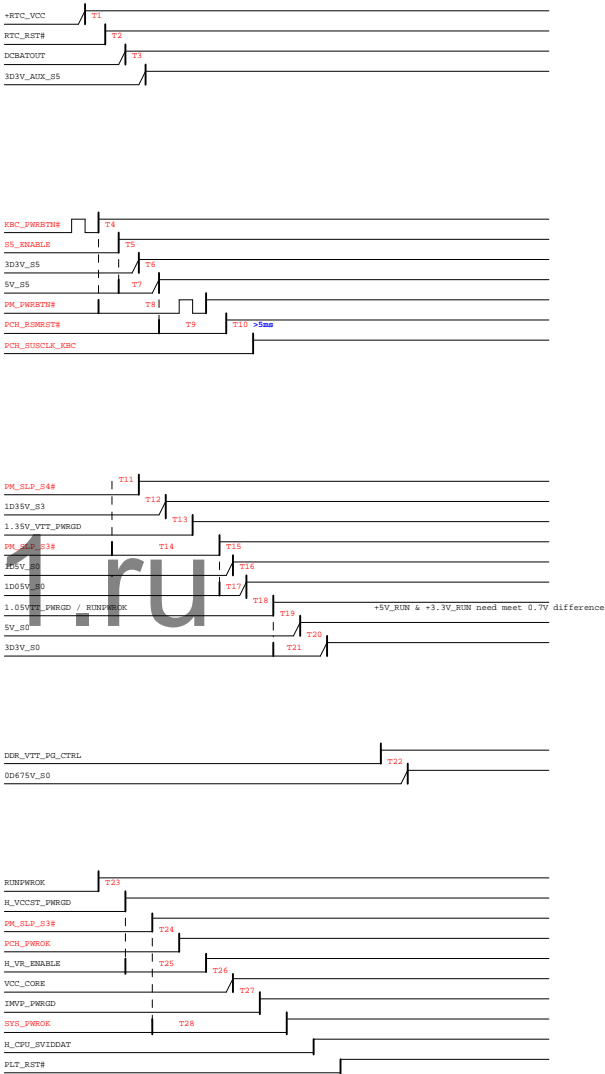
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Red printings:KBC GPIO involved



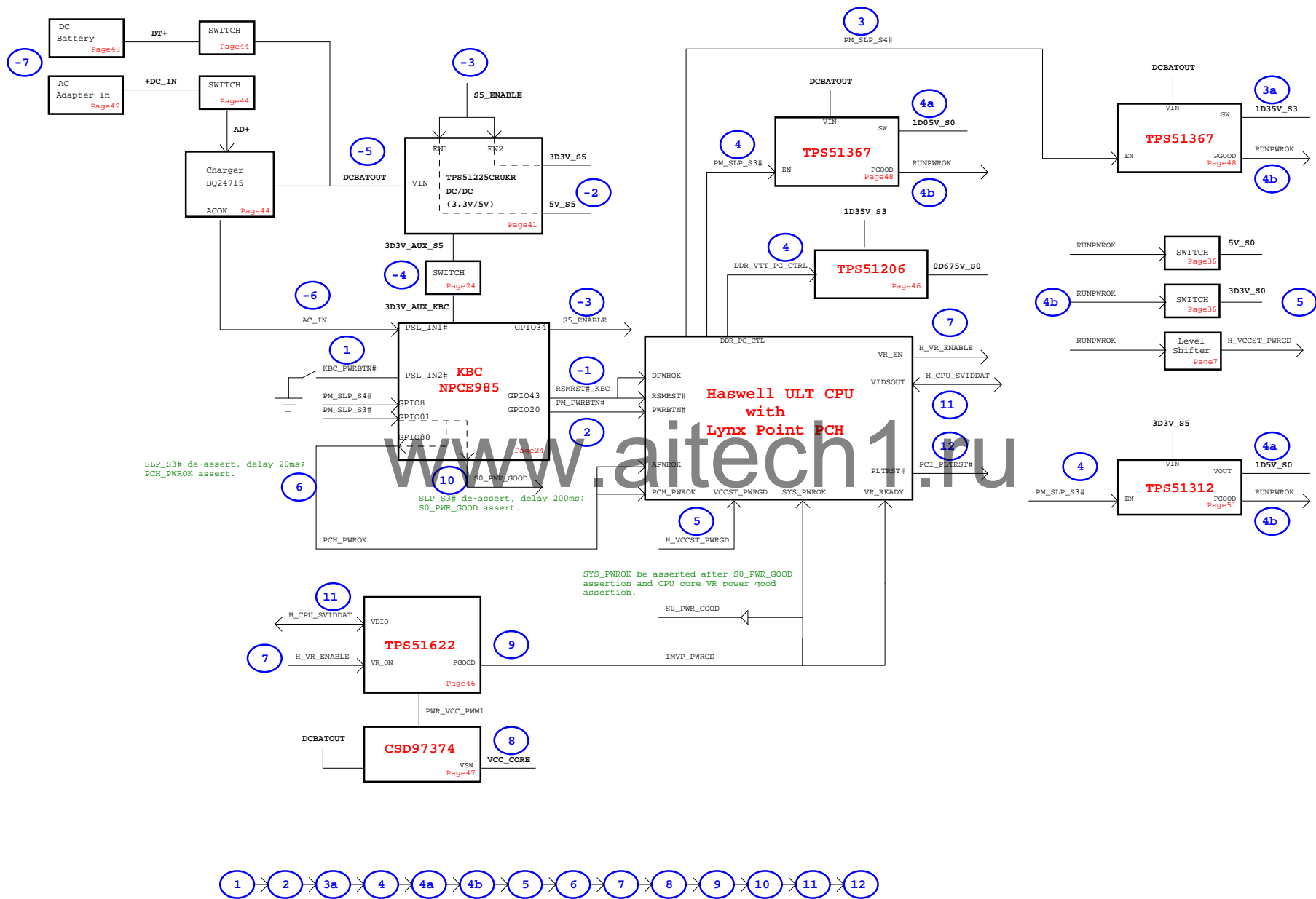
(DC mode)

Red printings:KBC GPIO involved

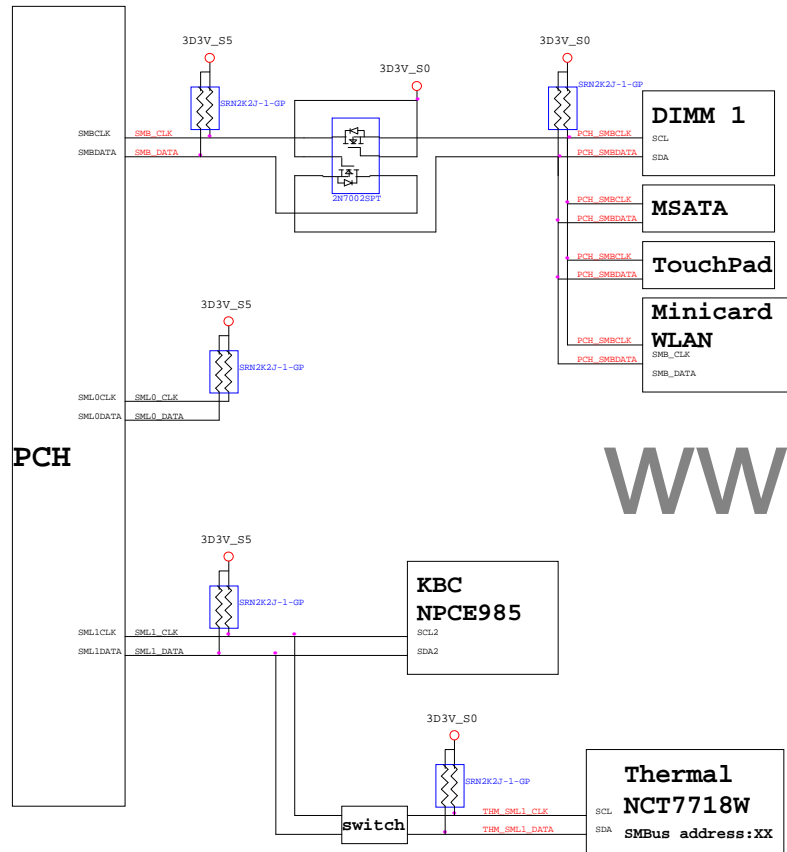


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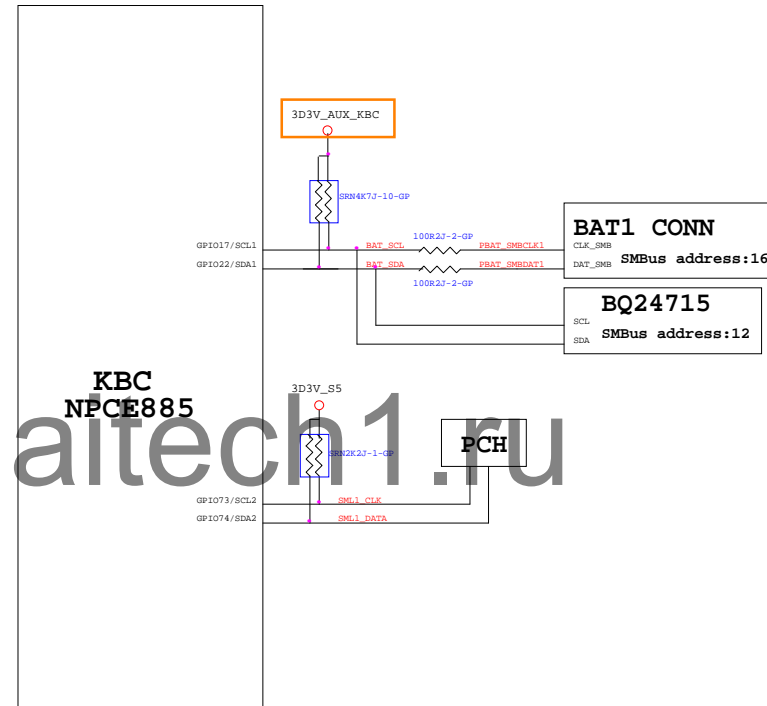
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



PCH SMBus Block Diagram

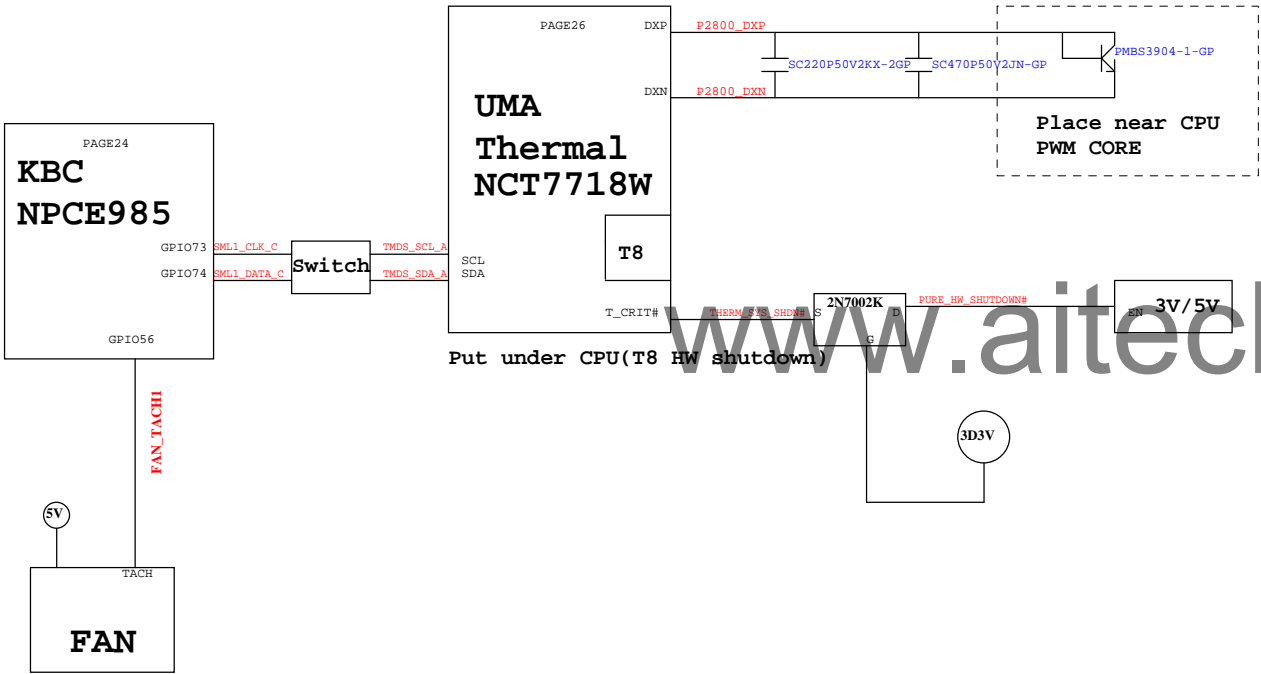


KBC SMBus Block Diagram



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Thermal Block Diagram



Audio Block Diagram

